ARM processor implementation

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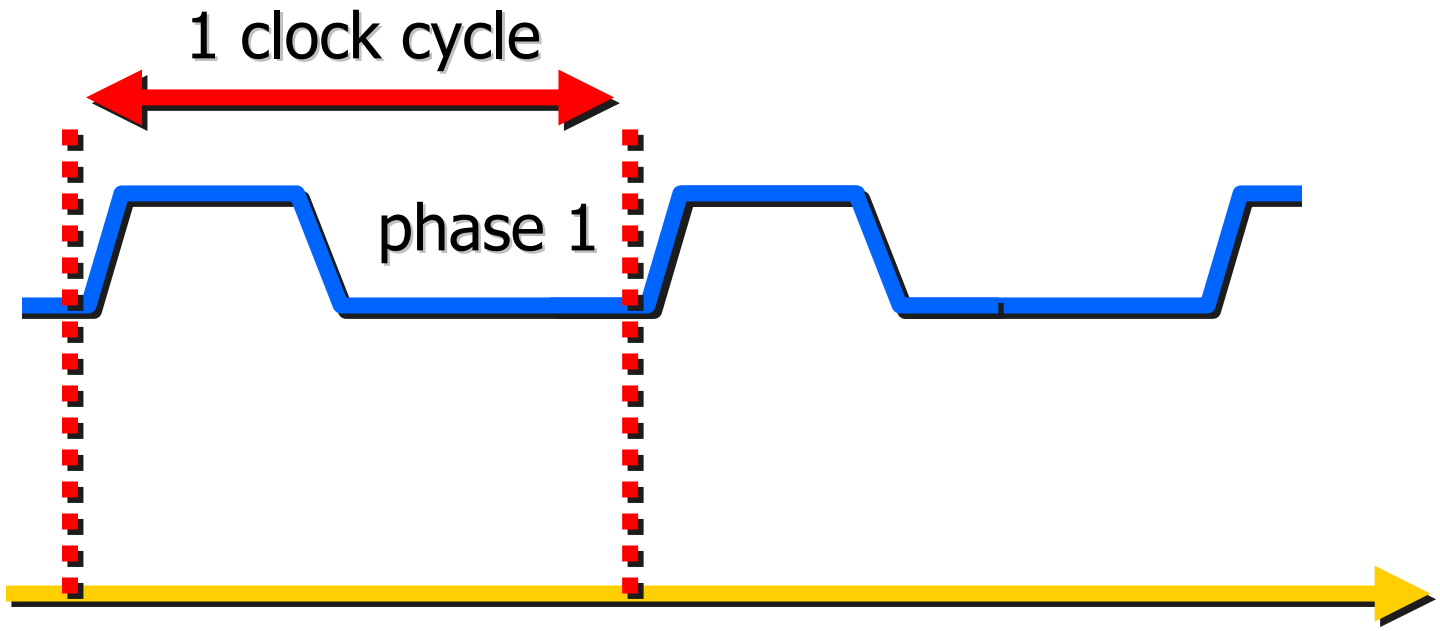

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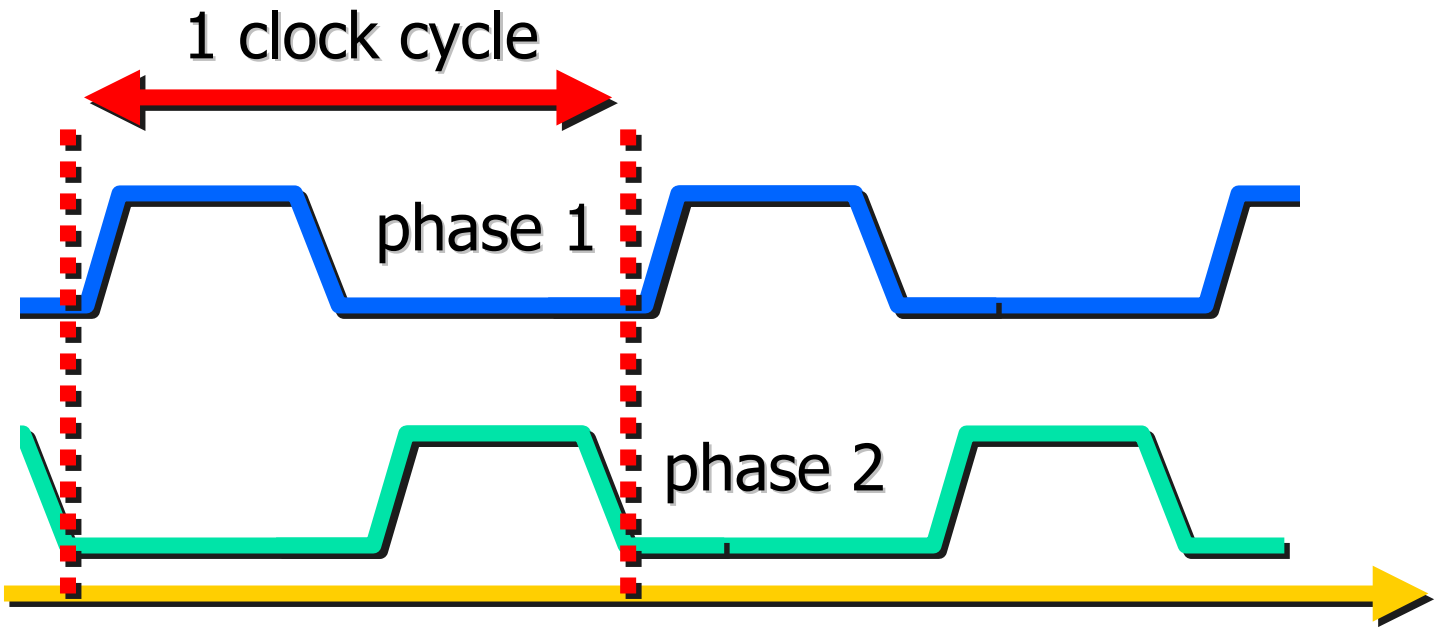
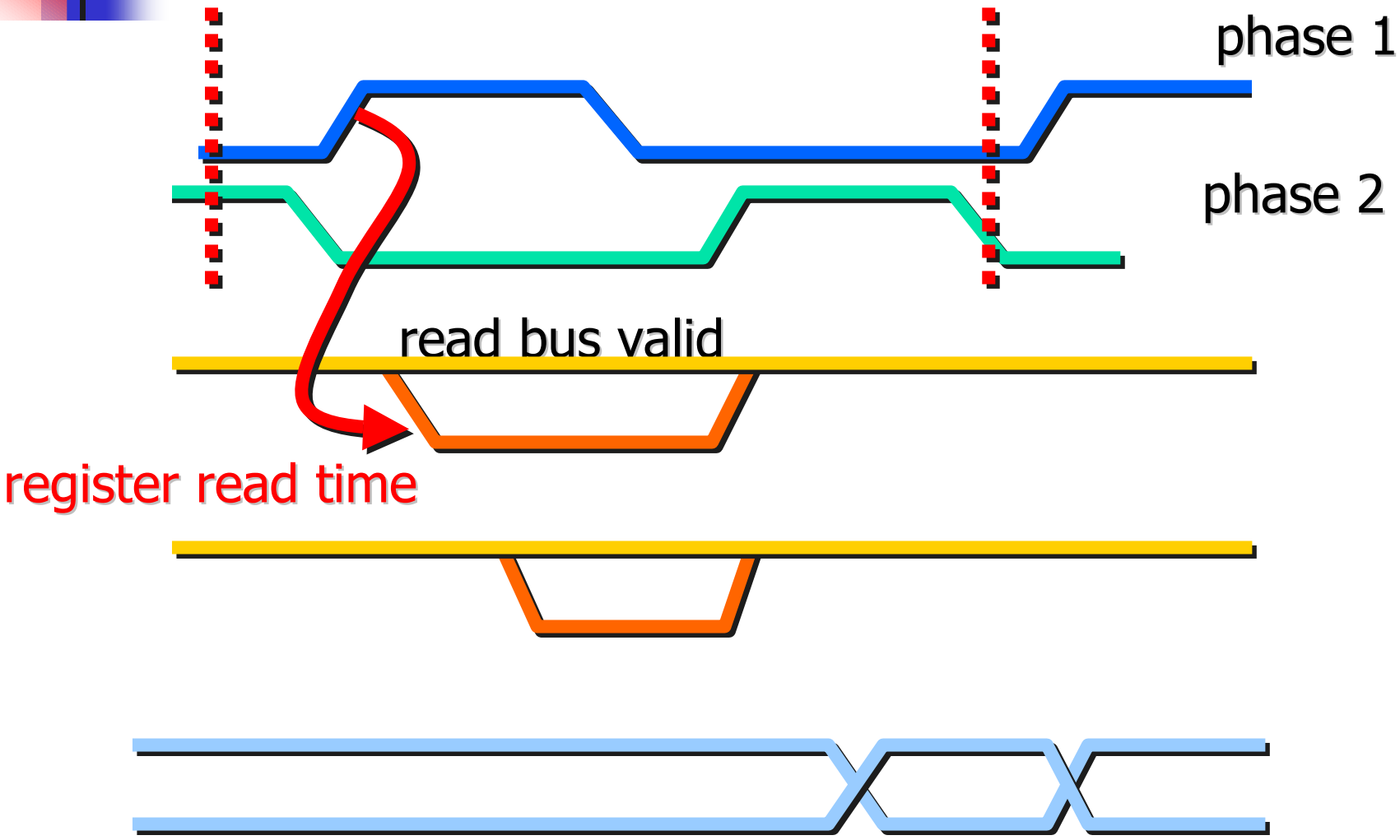


ARM data path timing



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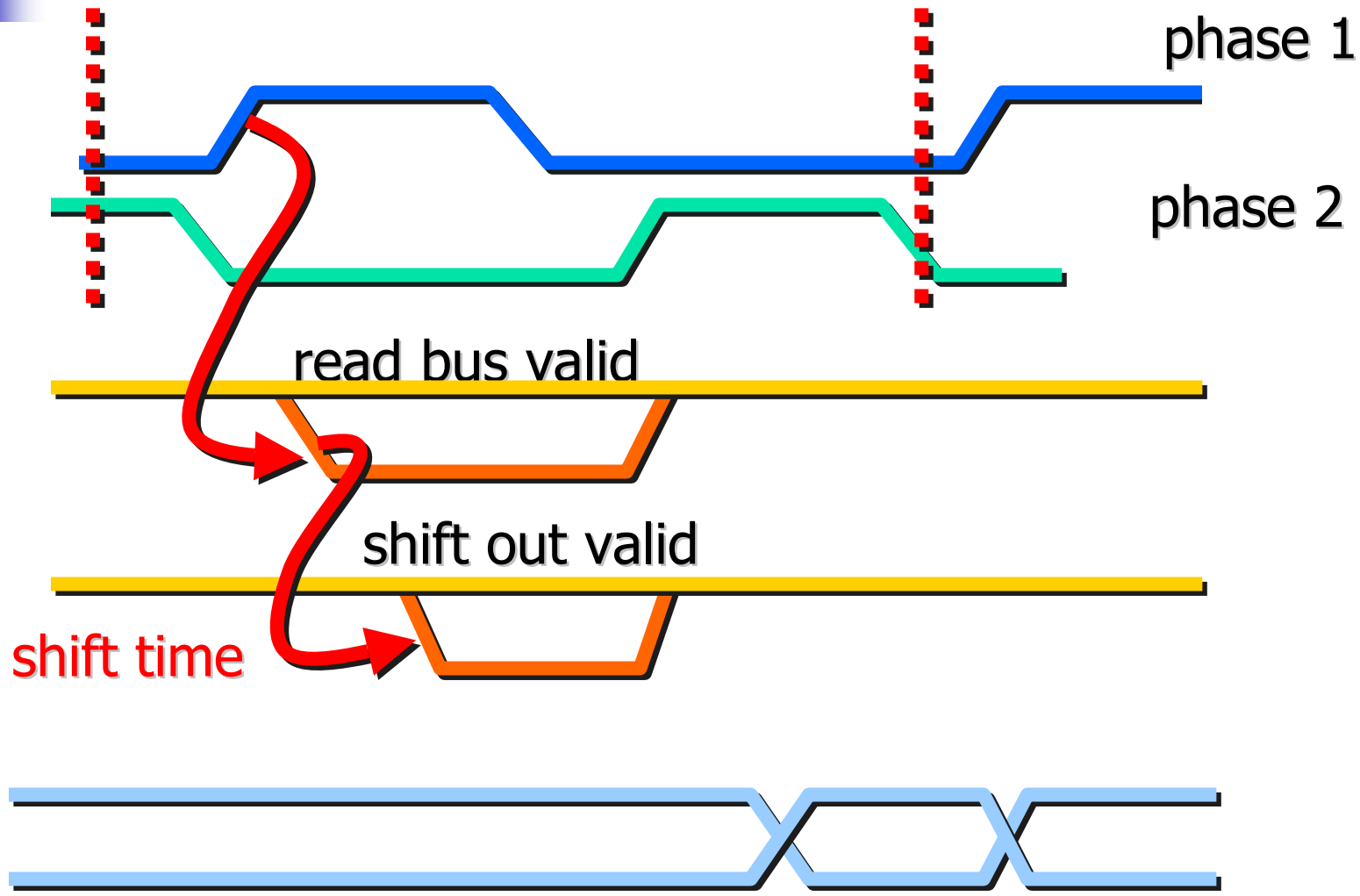

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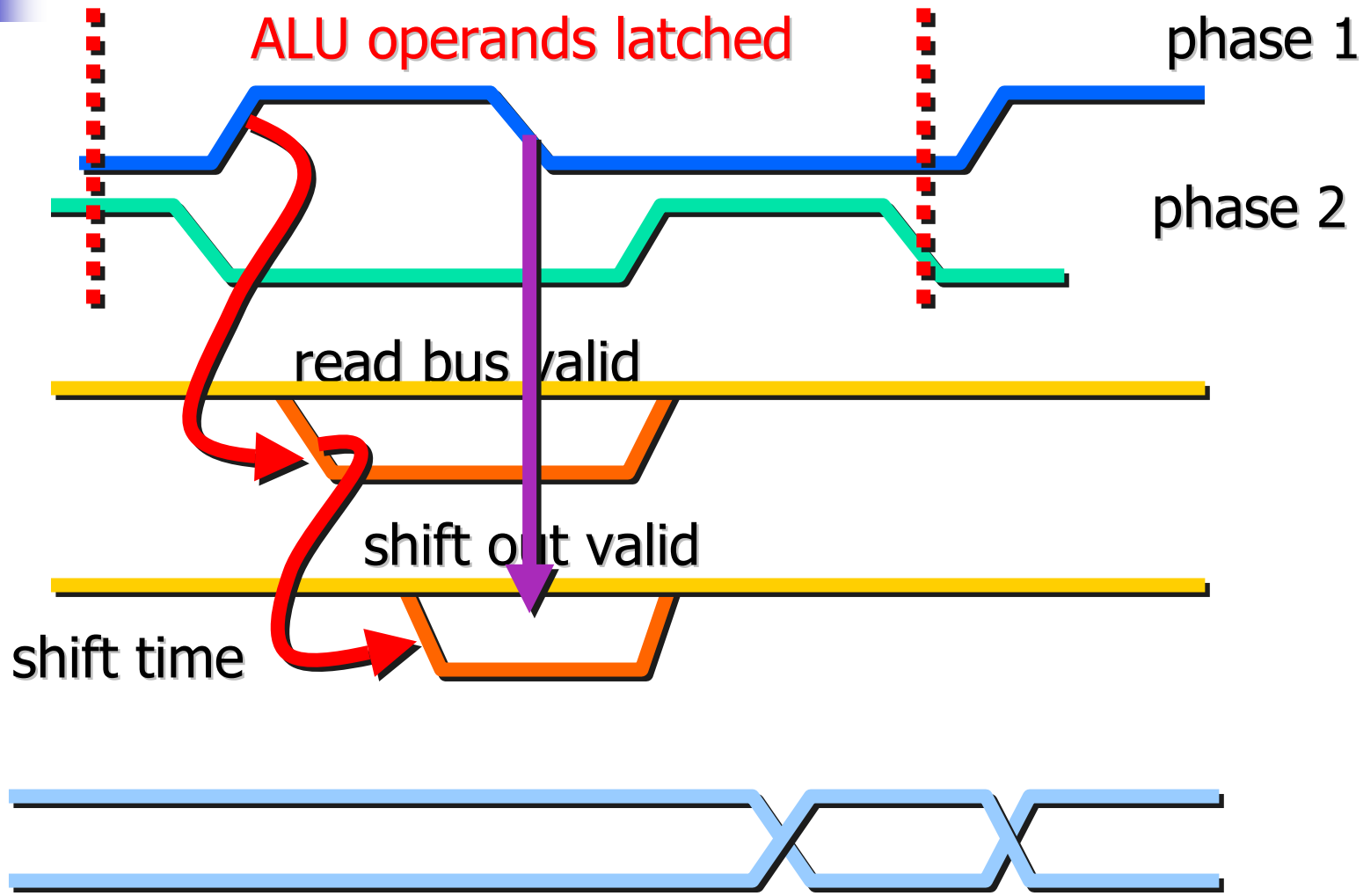

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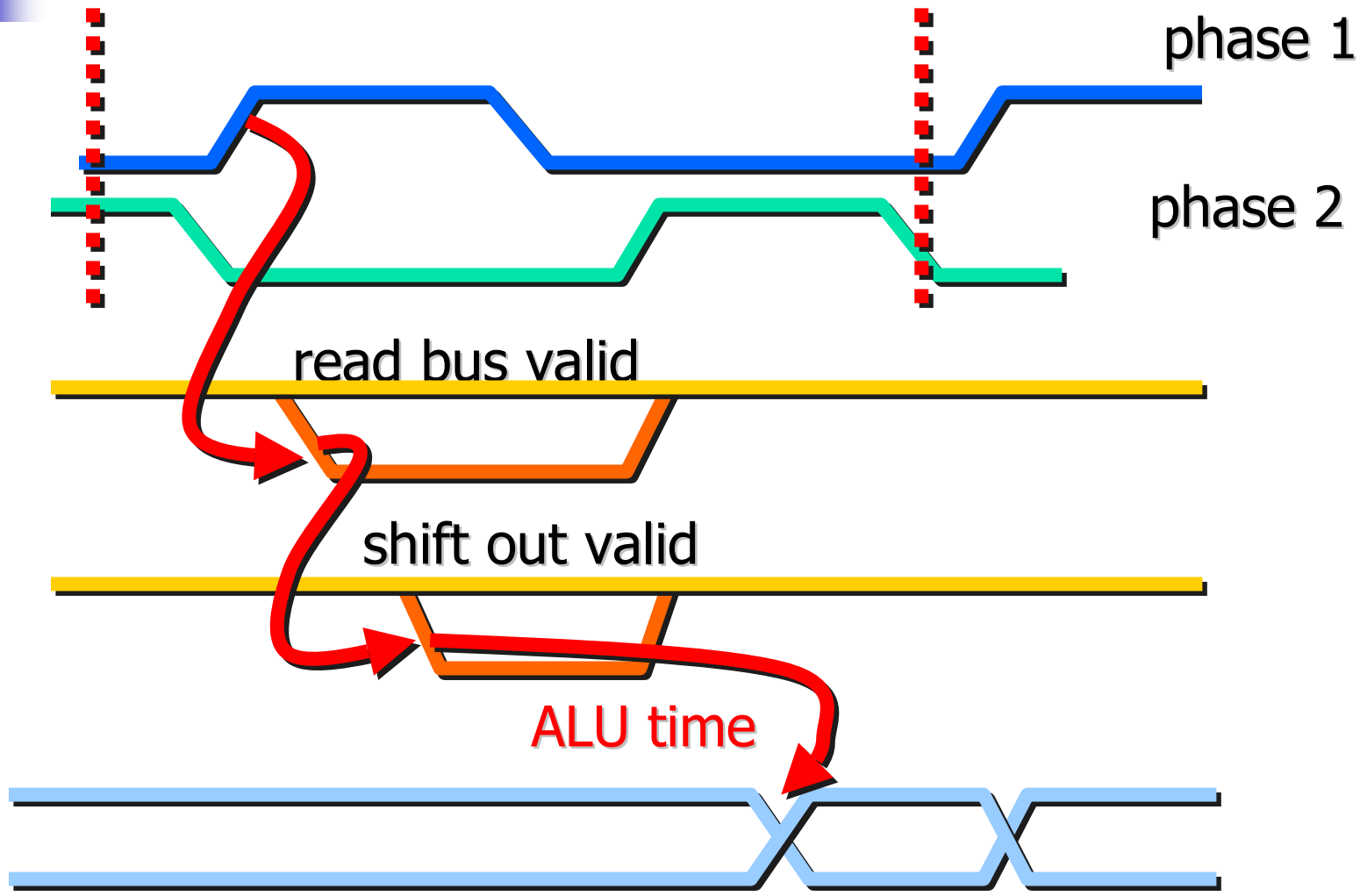

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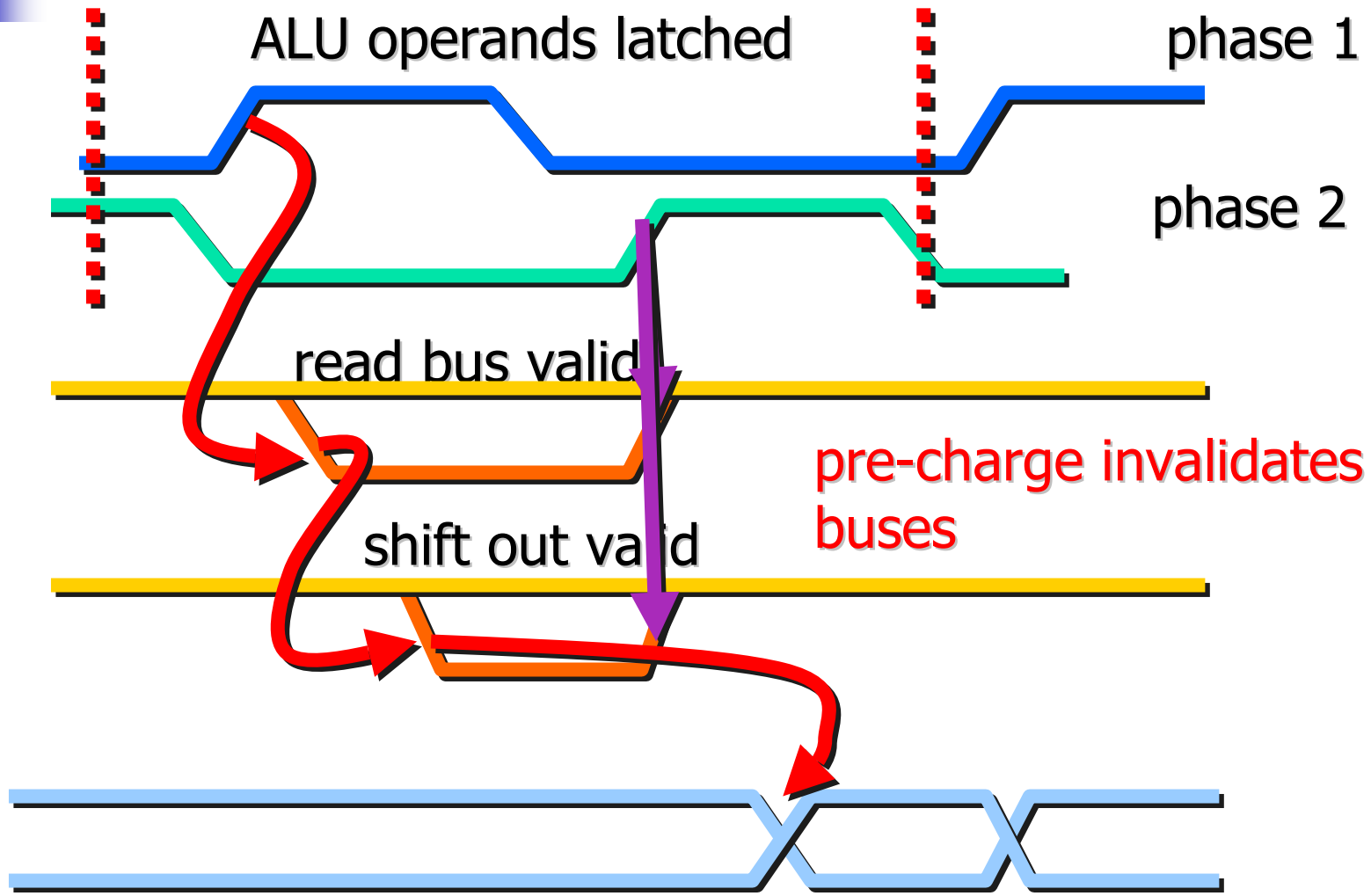

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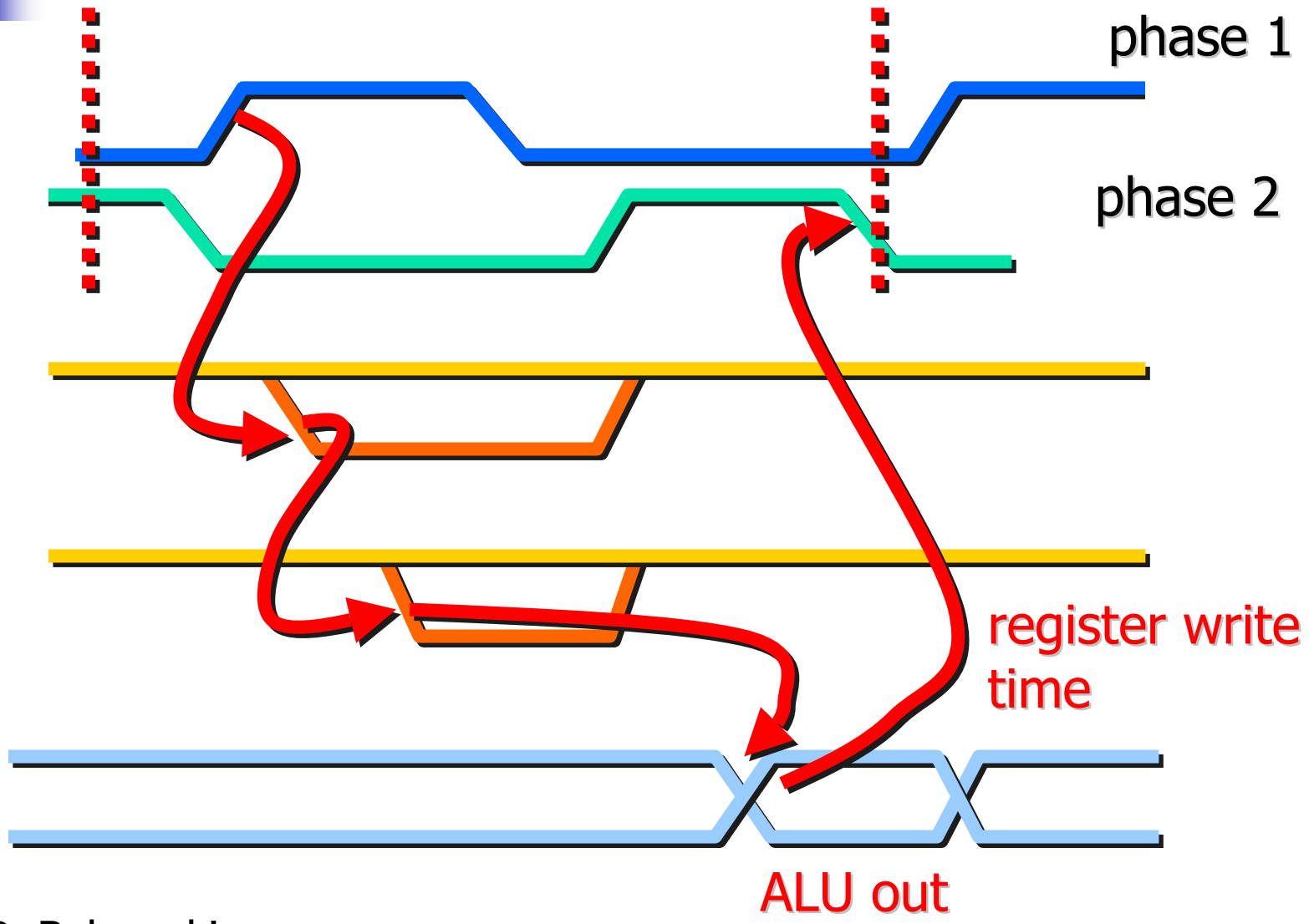

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- the shifter delay
- the ALU delay
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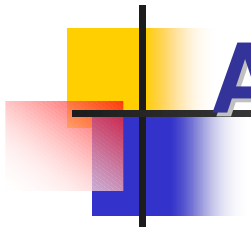

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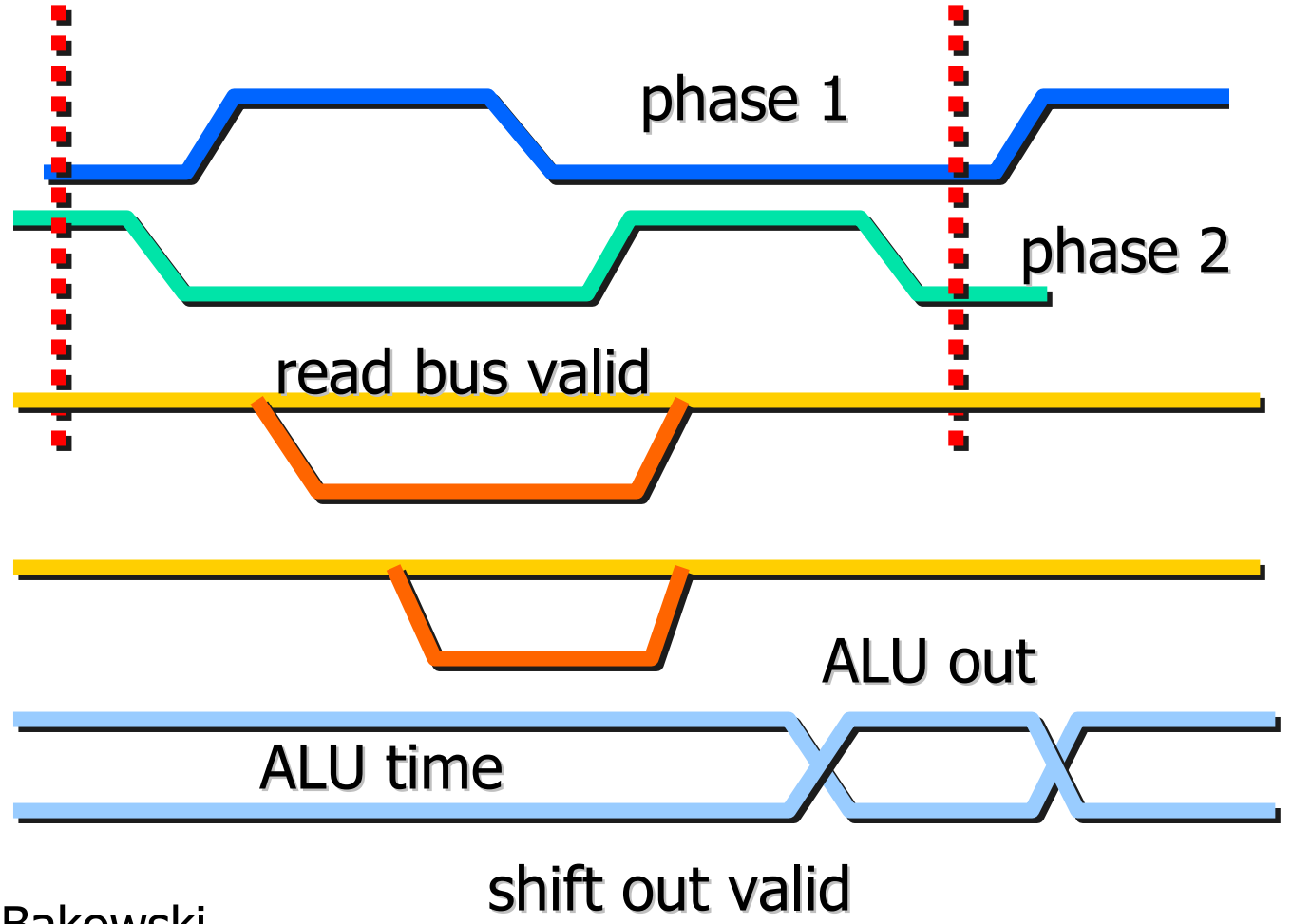
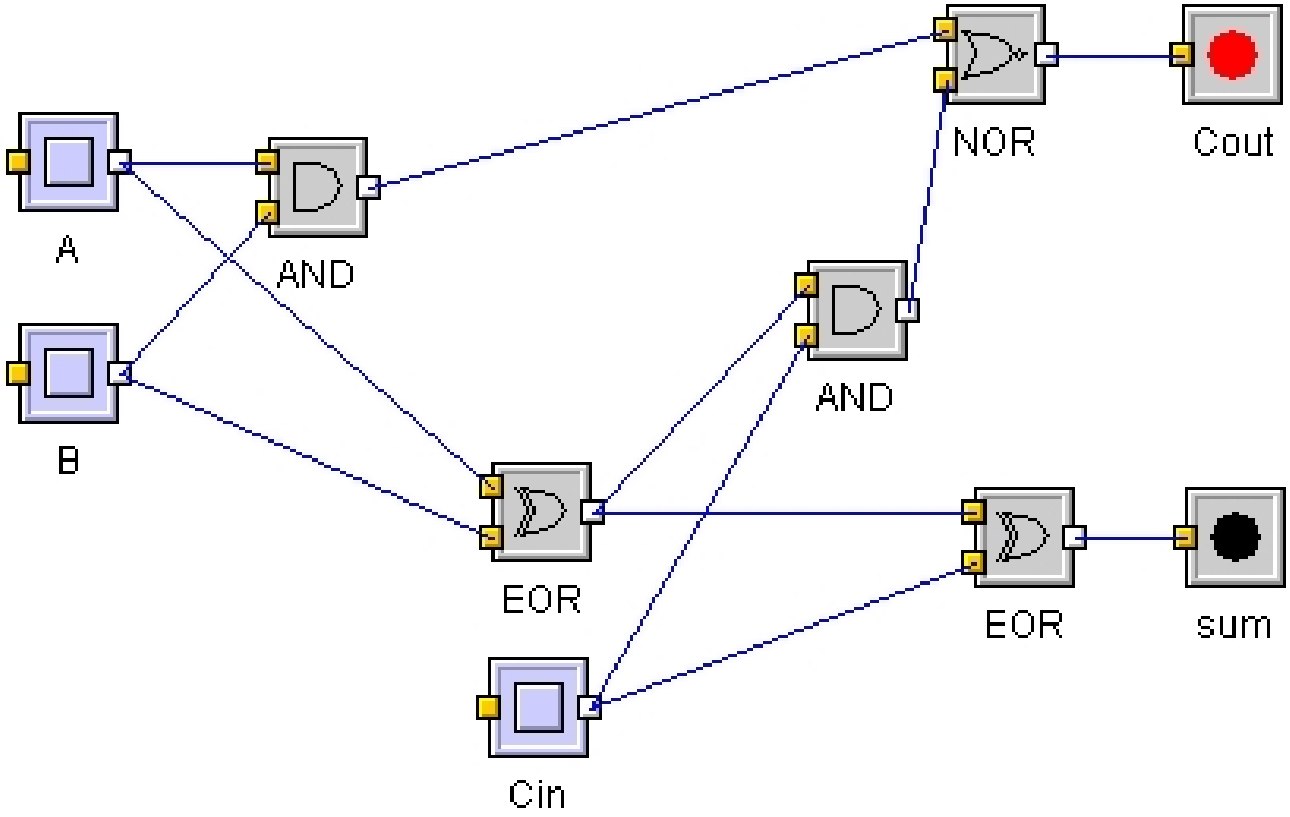
ARM data path timing

Timing in a 3-stage pipeline.



ARM 1 - adder design

ARM1 – the original ripple-carry adder:

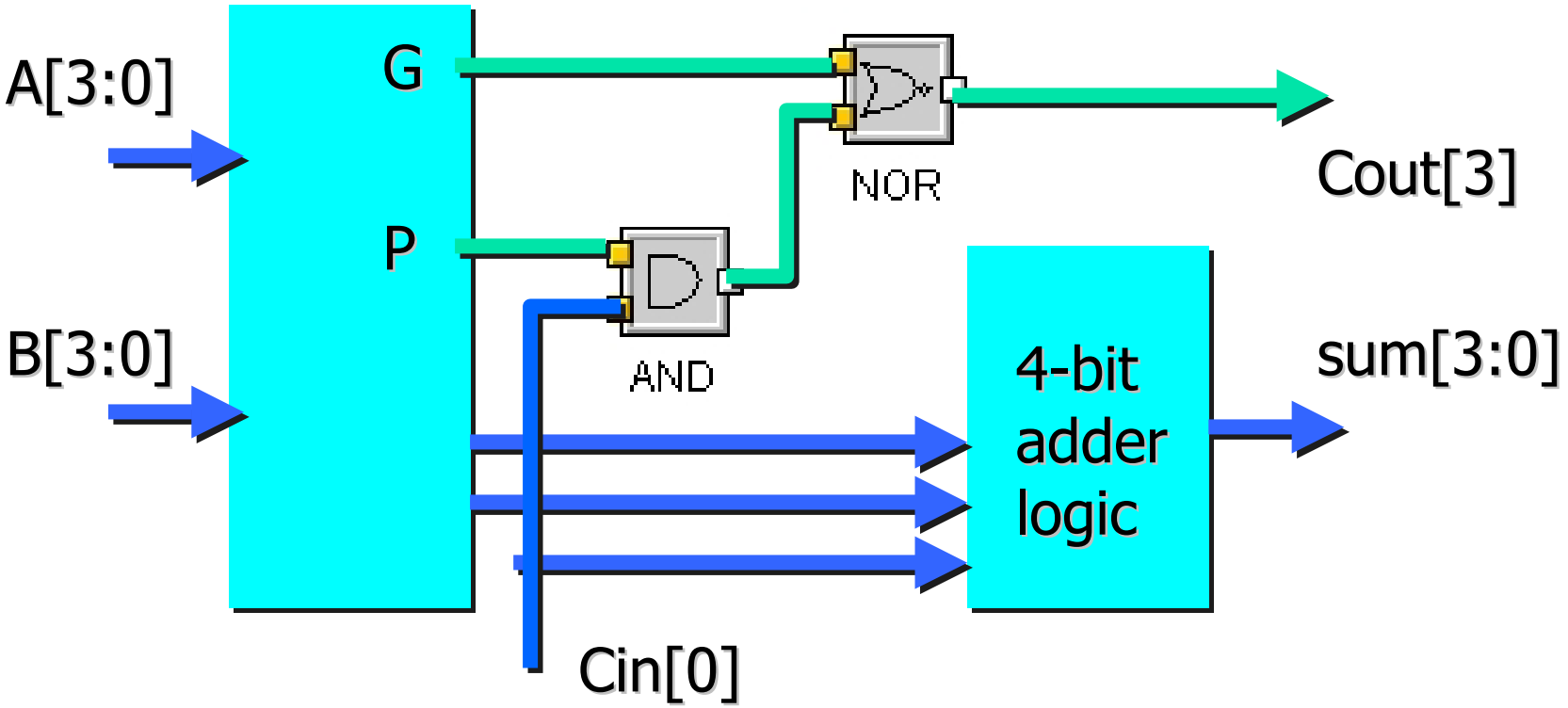


ARM 1 - adder design

Using CMOS and-or-invert gate for the carry logic and alternating and-or logic so that event bits use the circuit shown and odd bits use the dual circuit with inverted inputs and outputs and and-or gates swapped around, the worst-case carry path is 32 gates long.

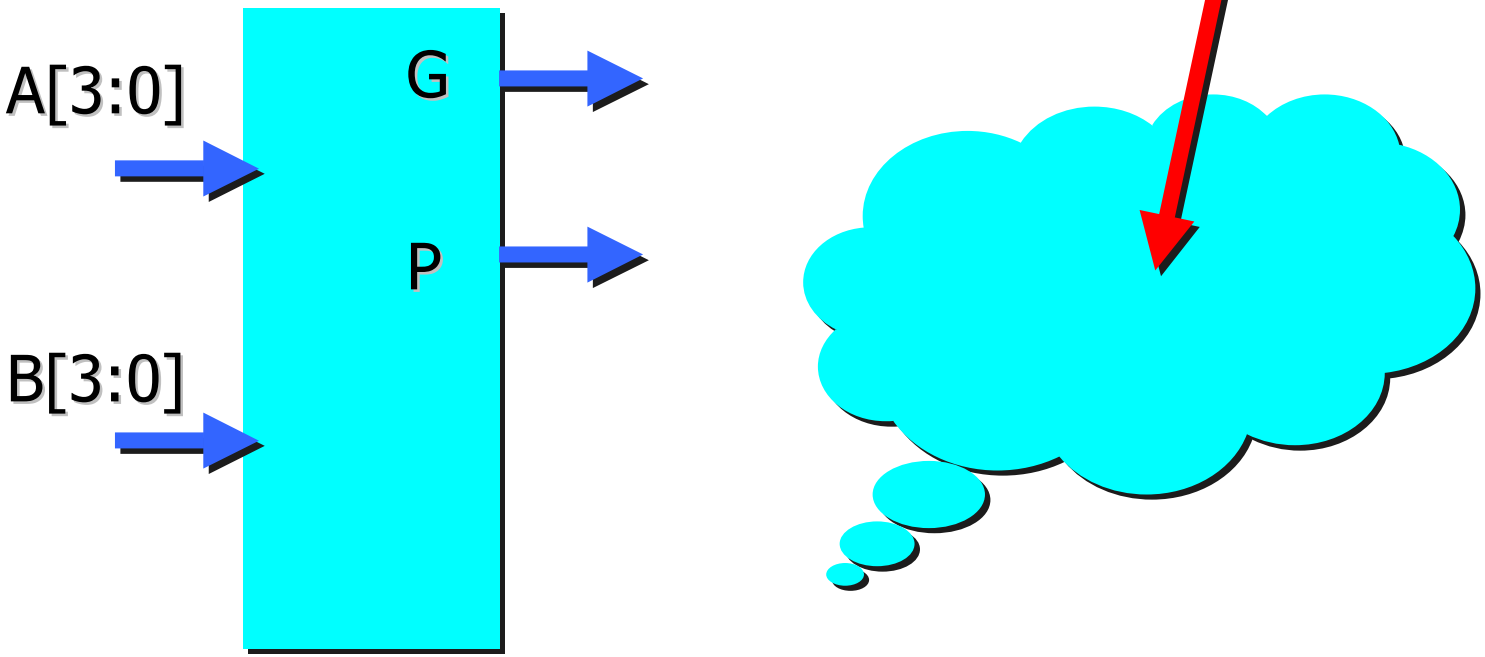
ARM 2 - adder design

To reduce the propagation path length ARM2 used a 4-bit carry look-ahead logic.

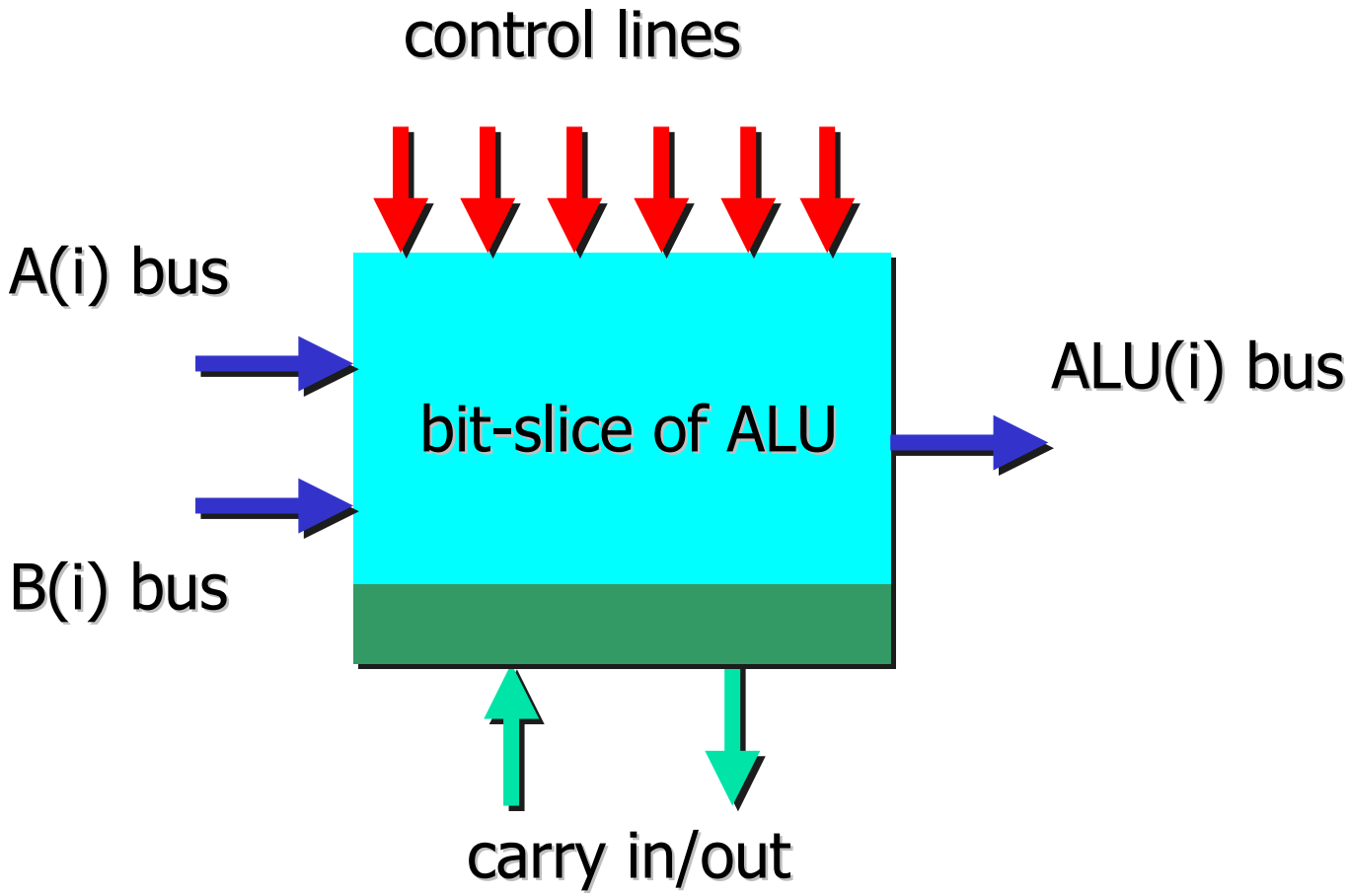


ARM 2 - adder design

Exercise: Draw the logic scheme of the circuit for Generate and Propagate signals



ARM 2 - ALU design



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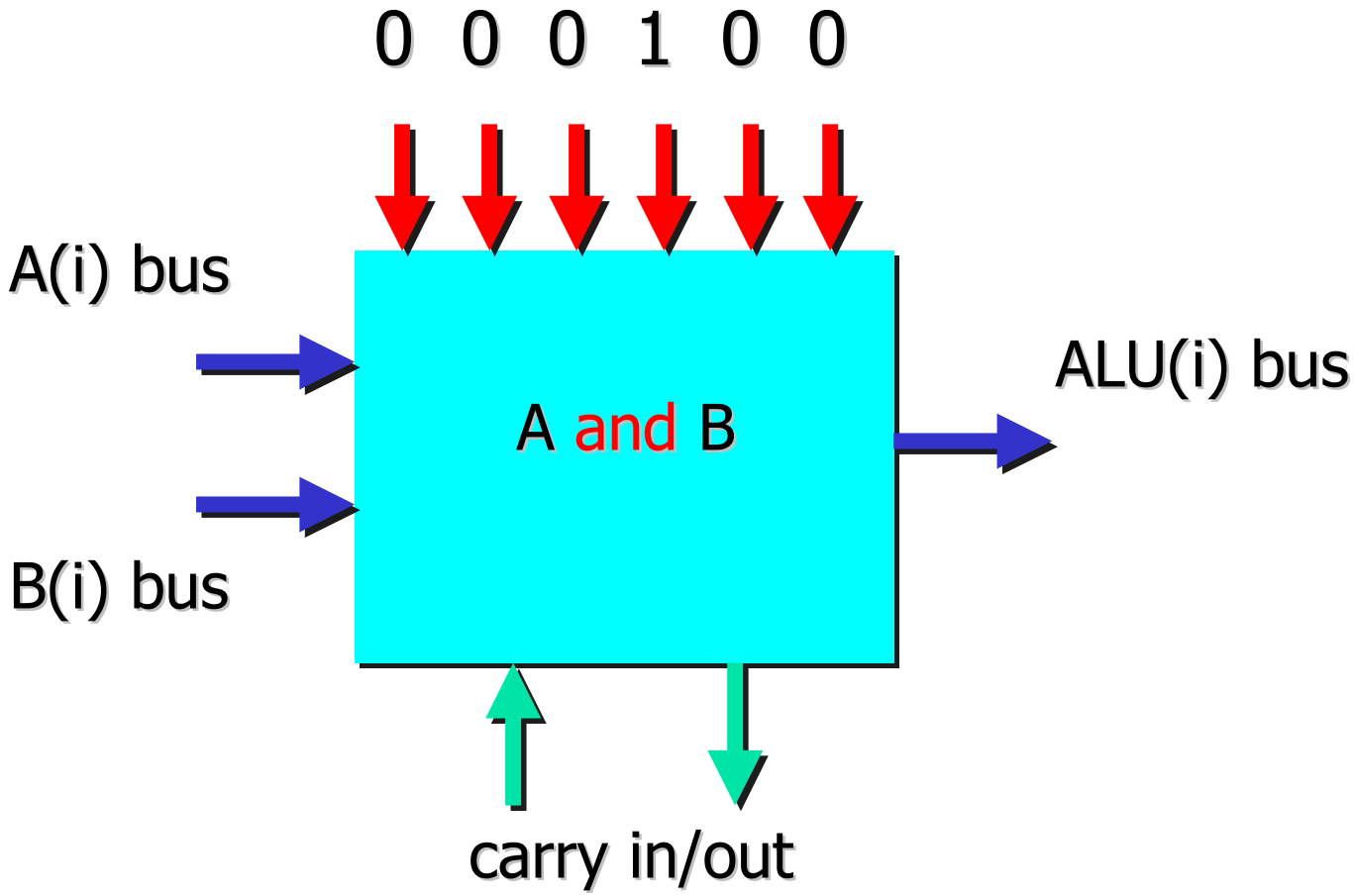

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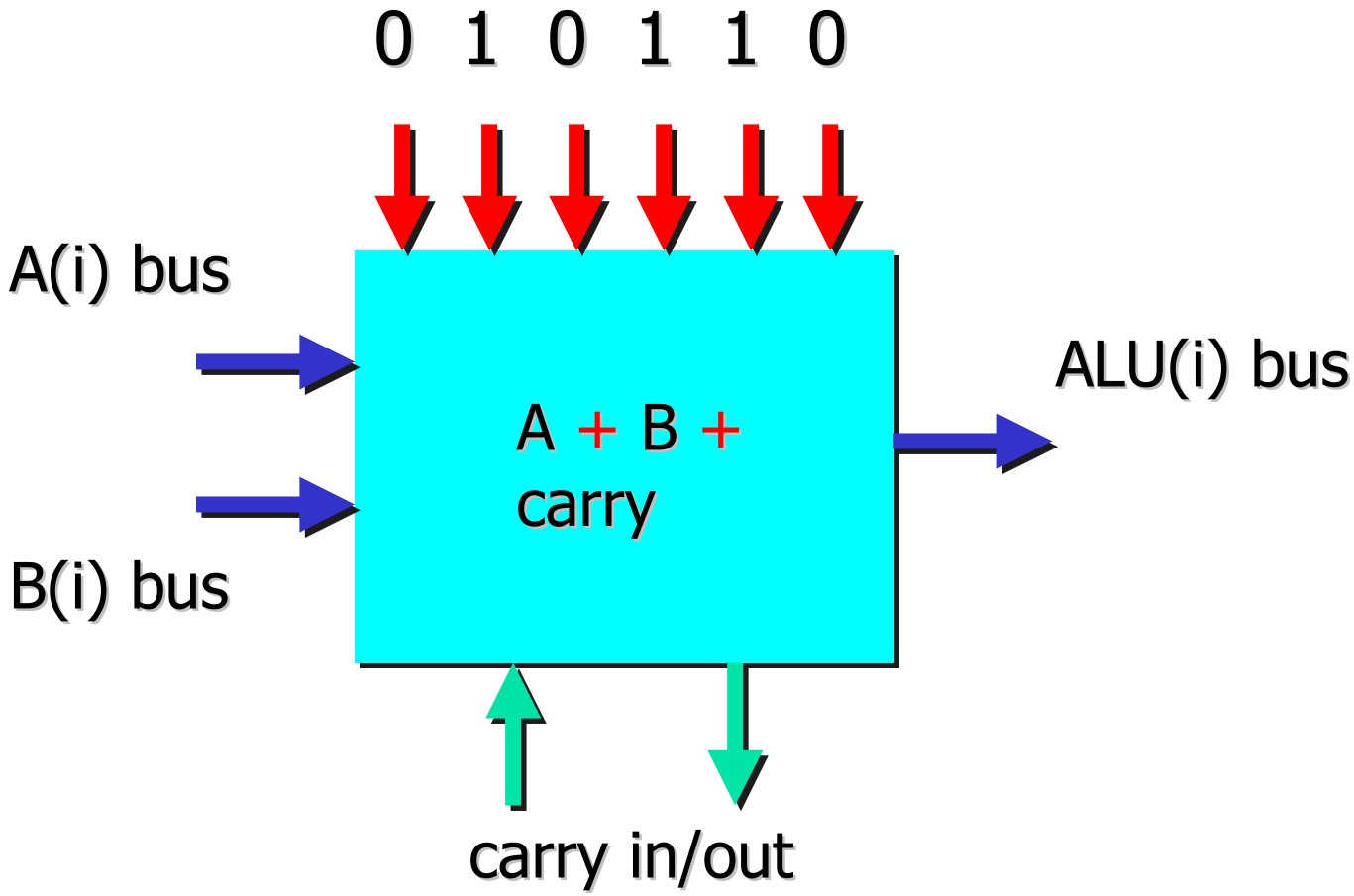

ARM 6 - adder design

The further reduction of the propagation time is provided by a carry-select adder implemented with ARM 6.

This form of adder computes the sums of various fields of the word for a carry-in both zero and one.

The final result is selected by using the correct carry-in value to control a multiplexer.

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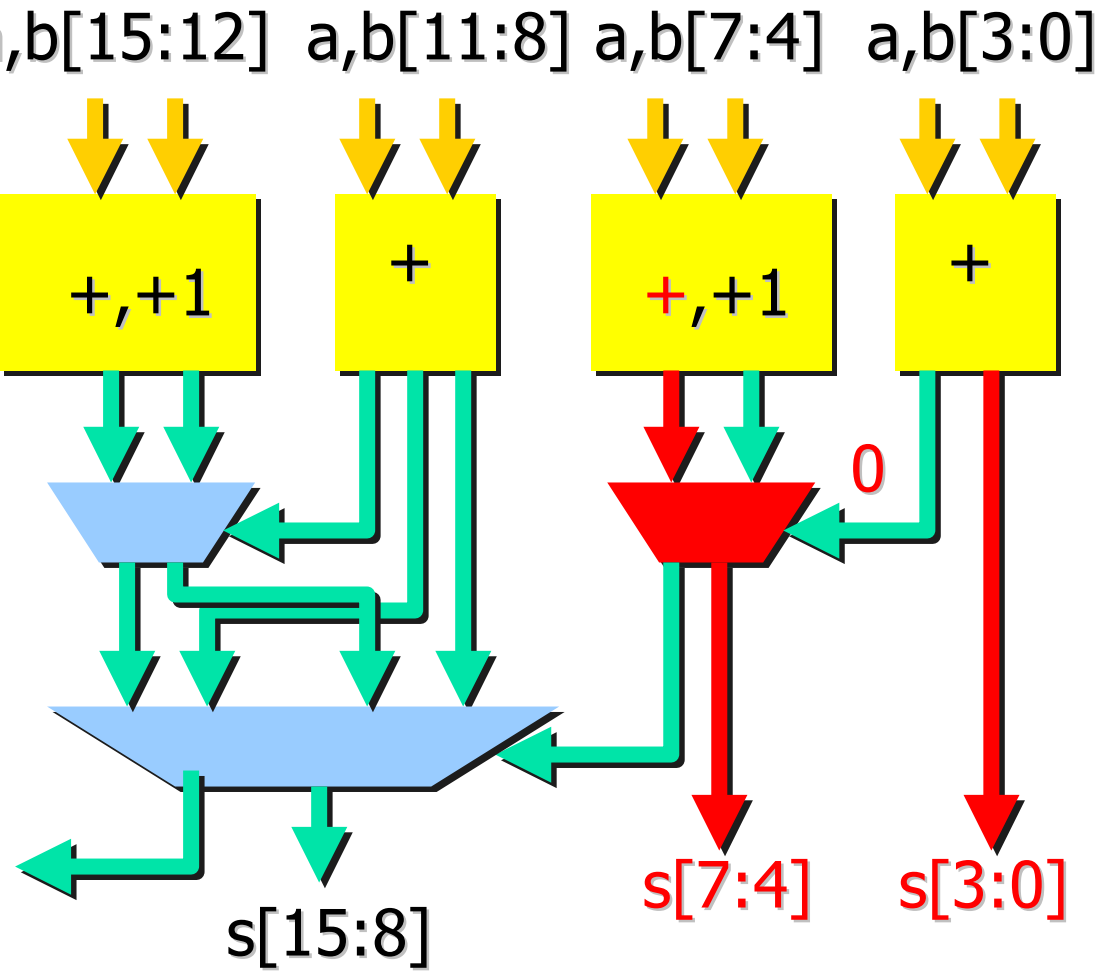

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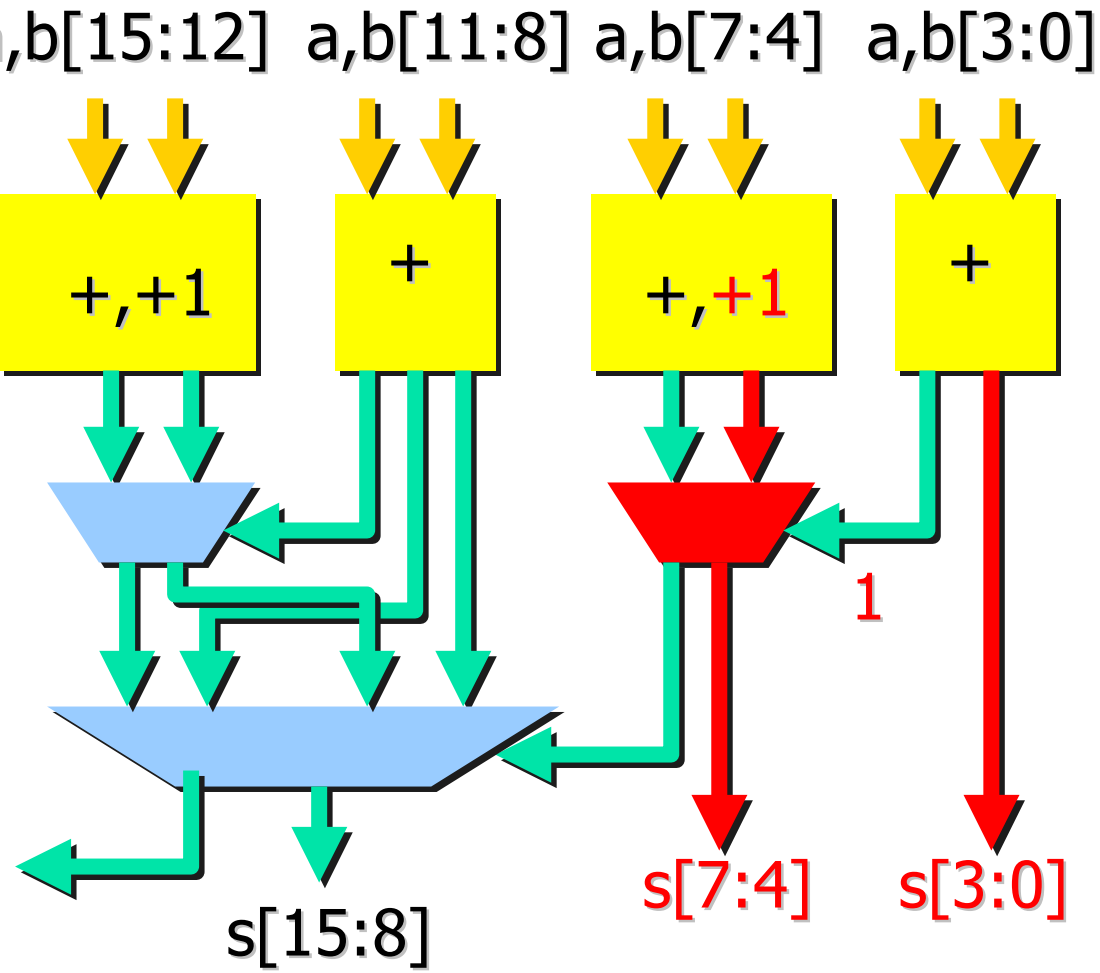

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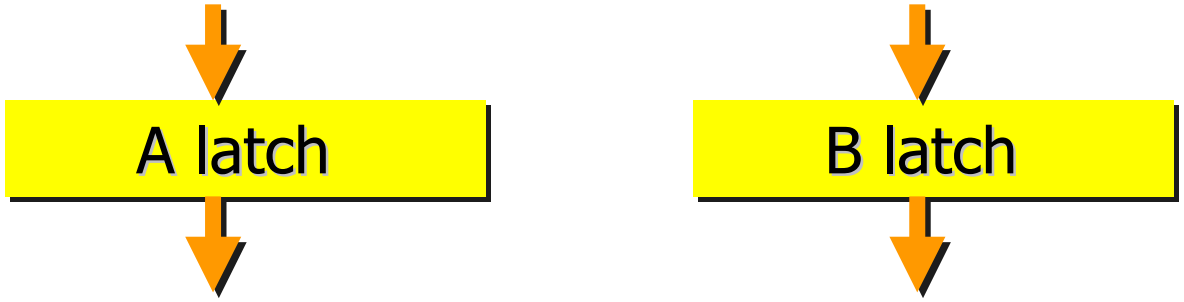

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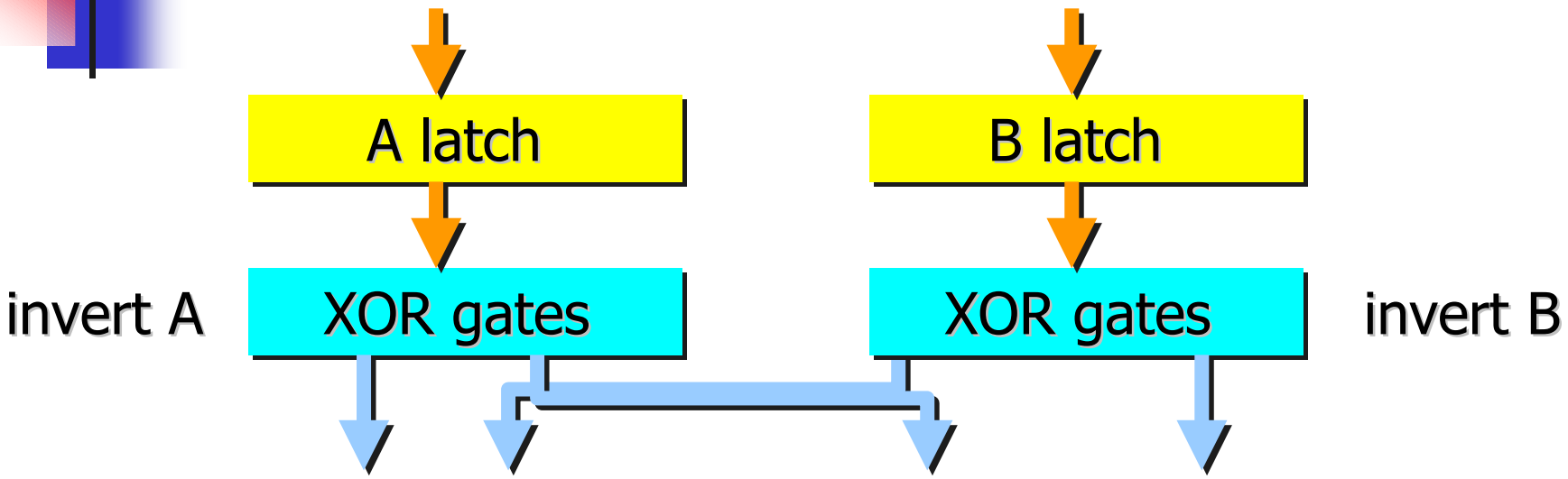

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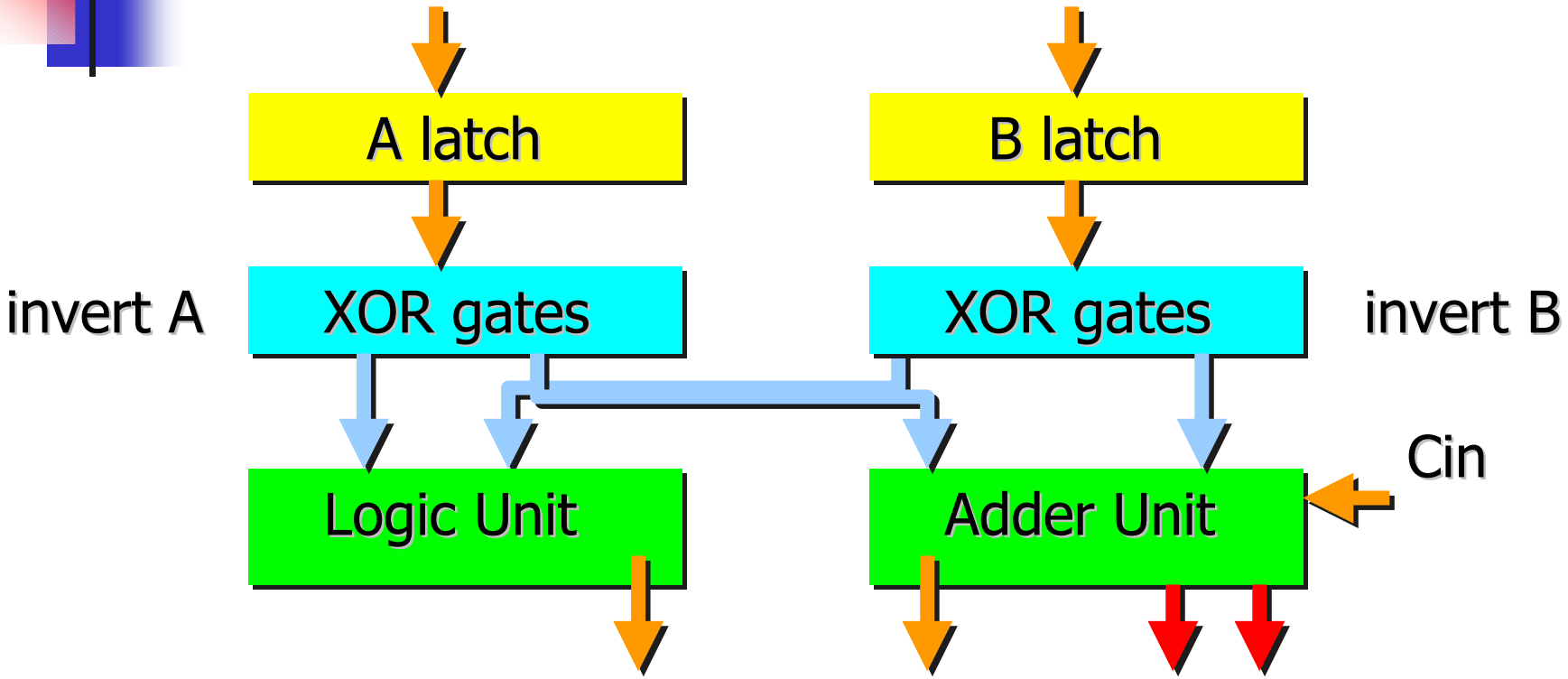

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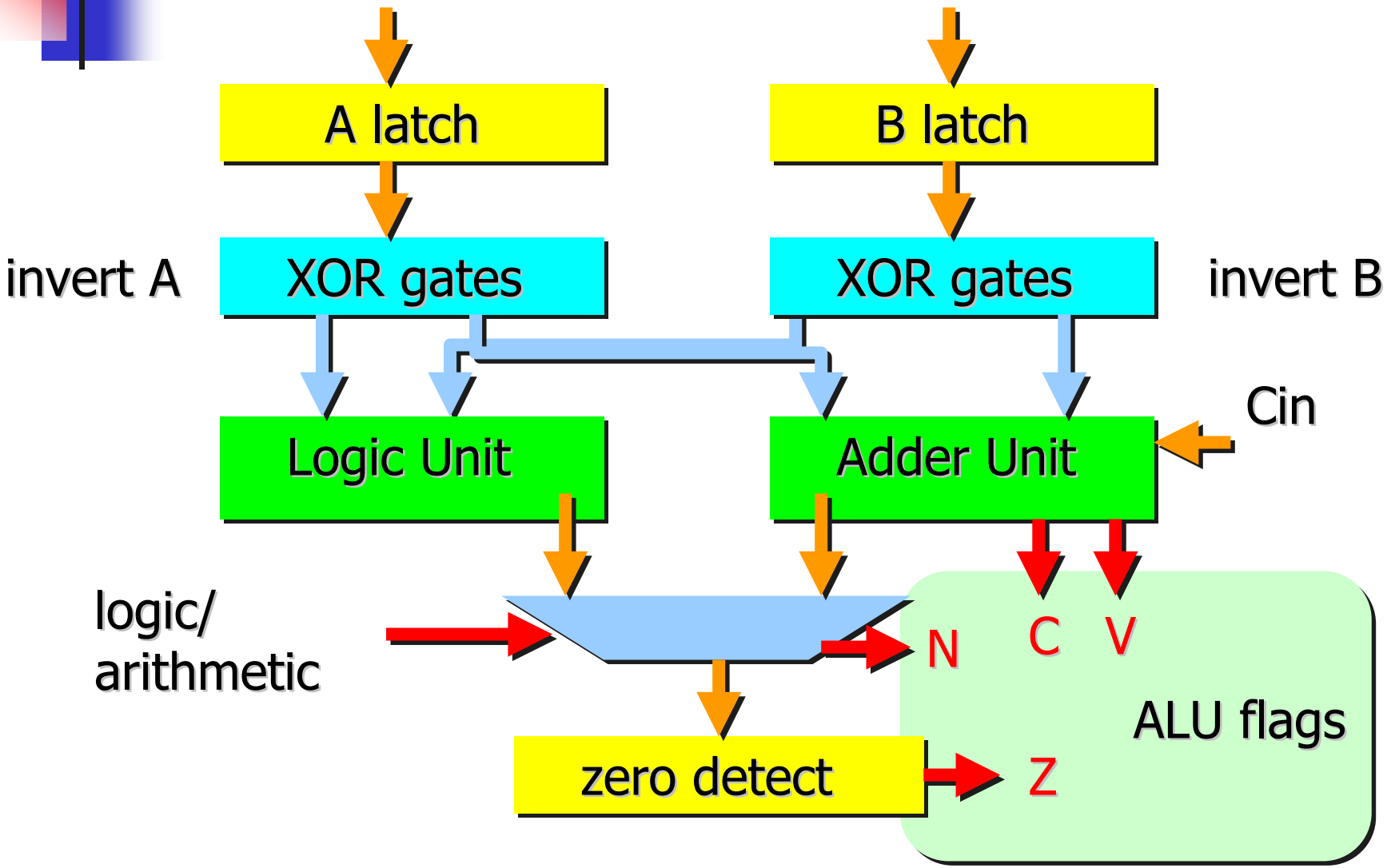

ARM barrel shifter

The shifter delay is critical because it is connected in series with ALU unit.

Therefore, it is implemented as a 32*32 cross-bar switch matrix where each input is steered directly to the appropriate output.

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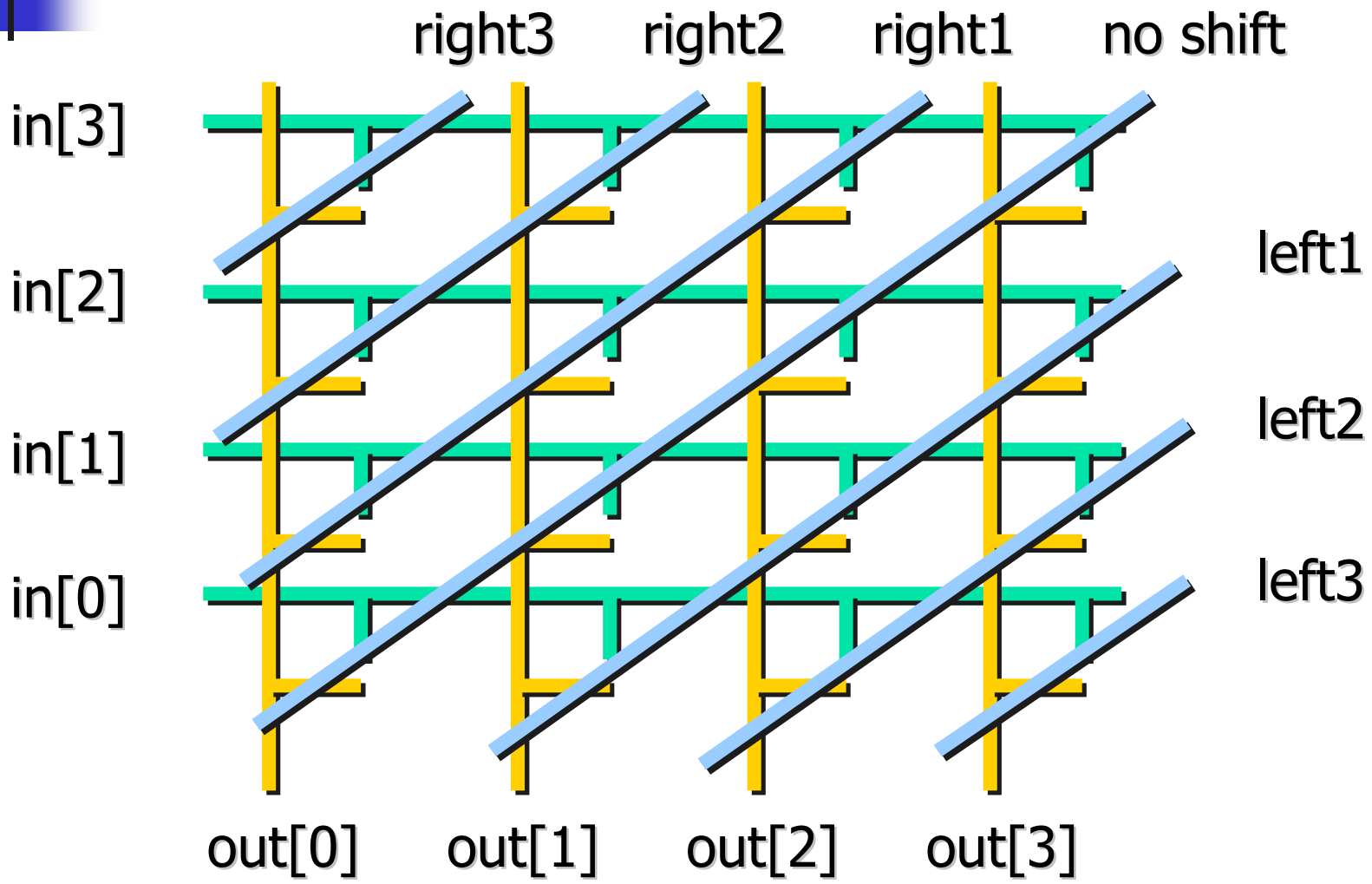

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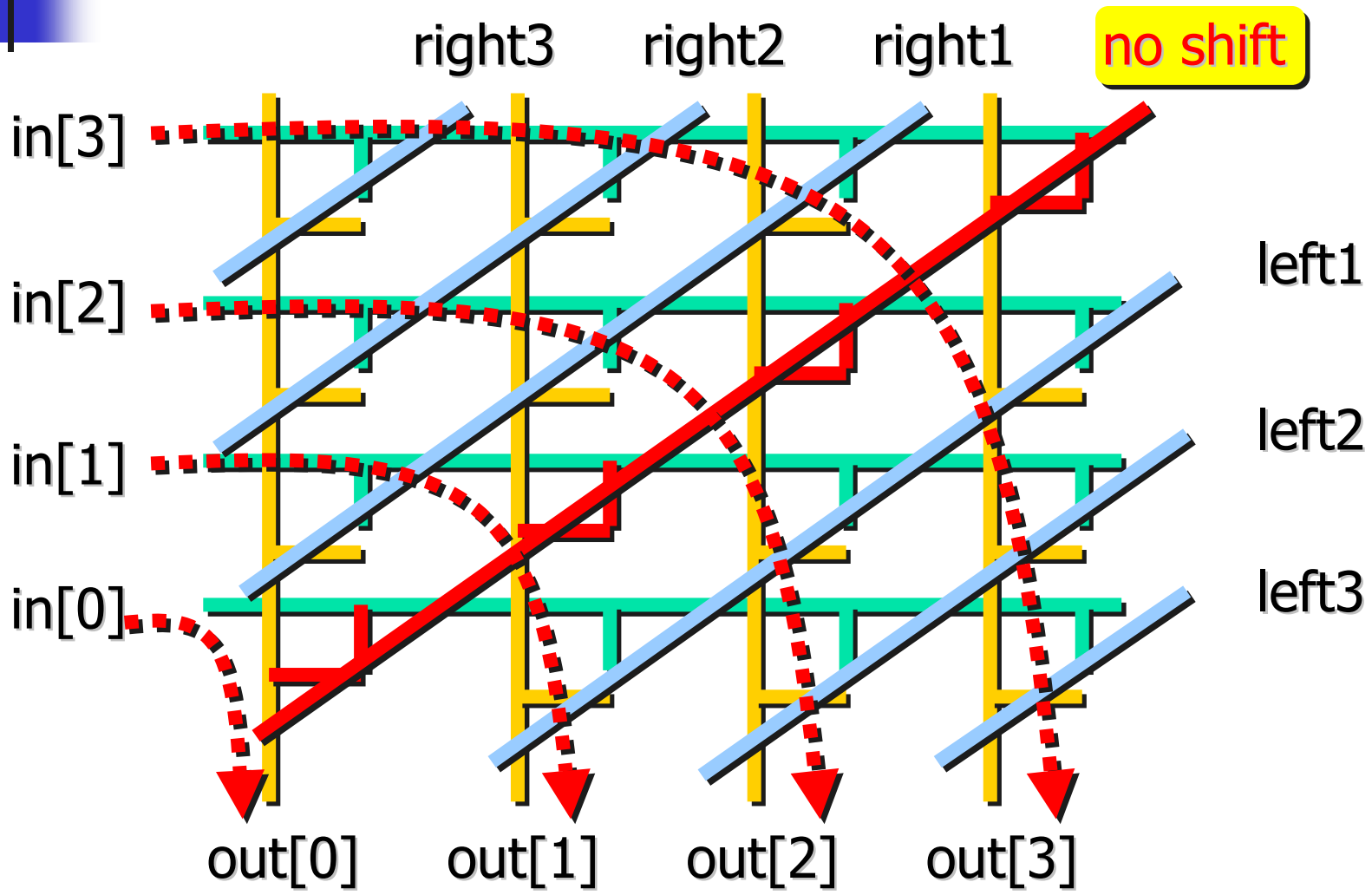

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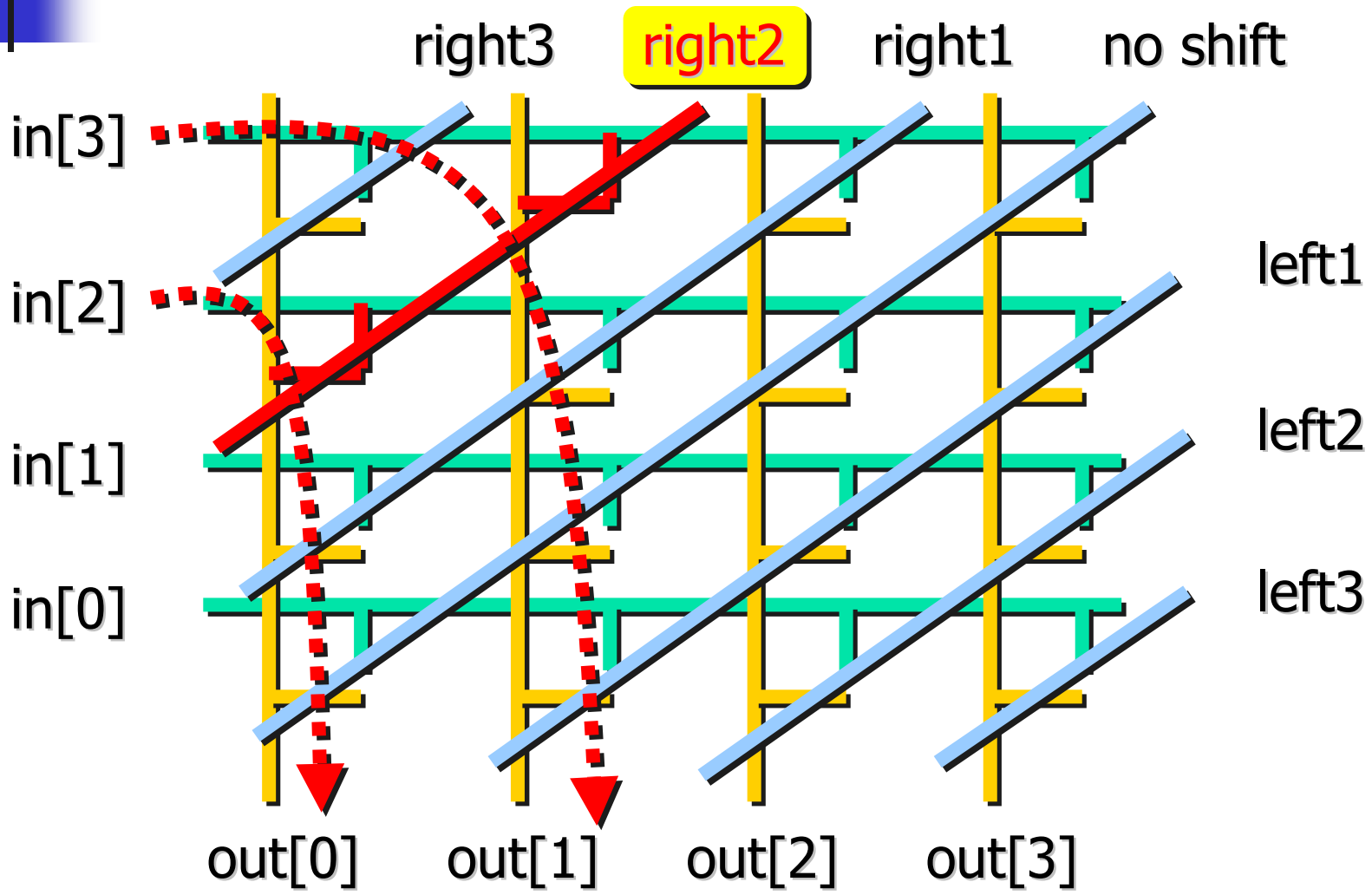

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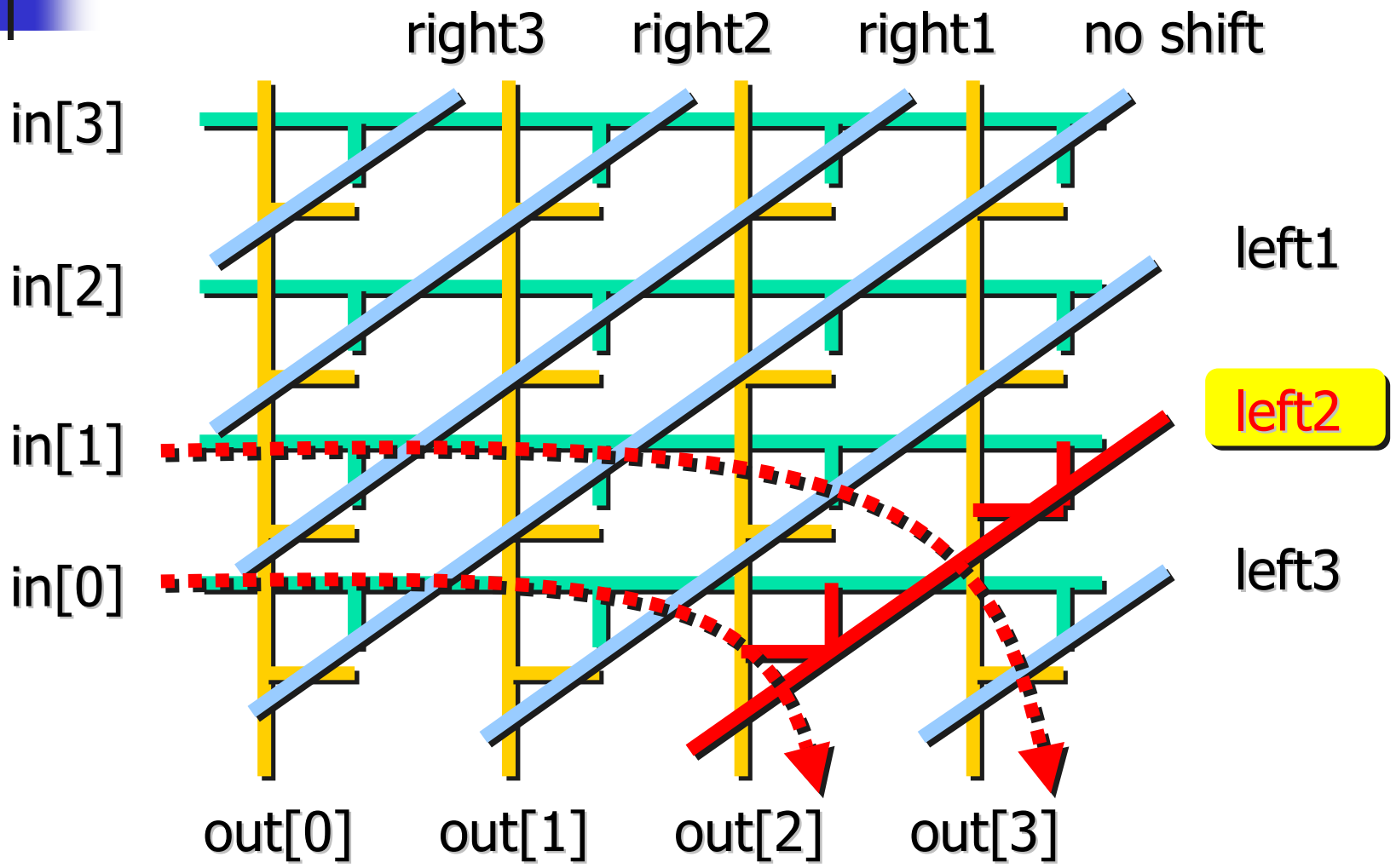

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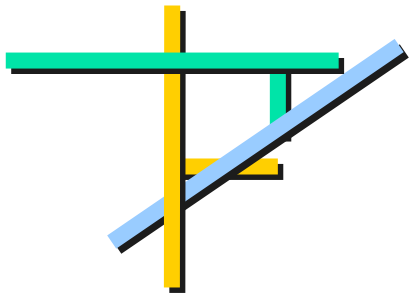
In the ARM the barrel shifter operates in negative logic where a '1' is represented as a potential near ground and a '0' by a potential near supply.

Pre-charging sets all the outputs to a logic '0' (supply potential), so those outputs that are not connected to any input during a particular switching operation remain at '0' giving the zero filling required by the shift semantics.



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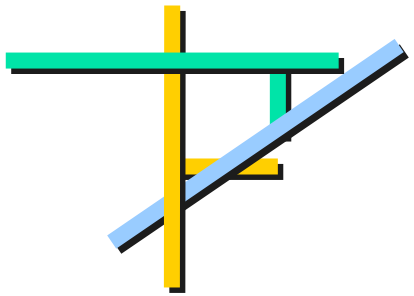

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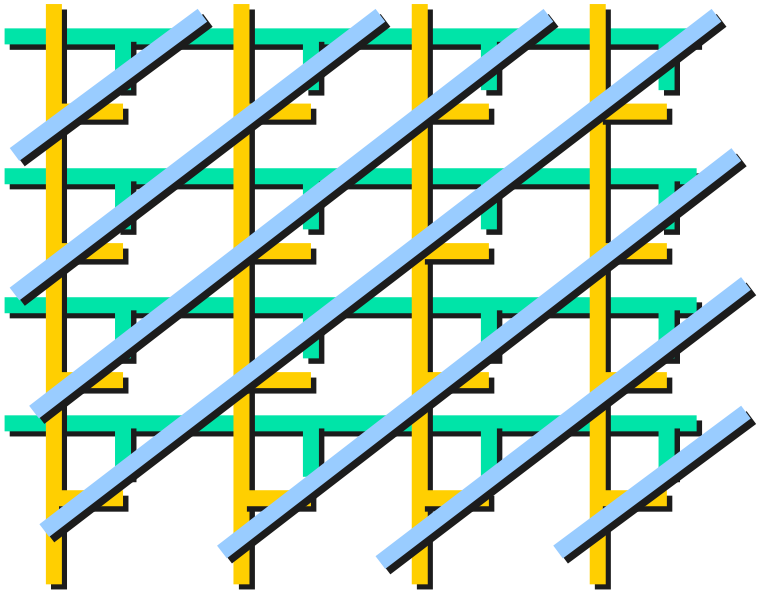
ARM barrel shifter - rotations

For rotate right function, the right shift diagonal is enabled together with the complementary shift diagonal.

For example, on the 4-bit matrix rotate right one bit is implemented using the ‘right1’ and the ‘left3’ (3=4-1) diagonals.



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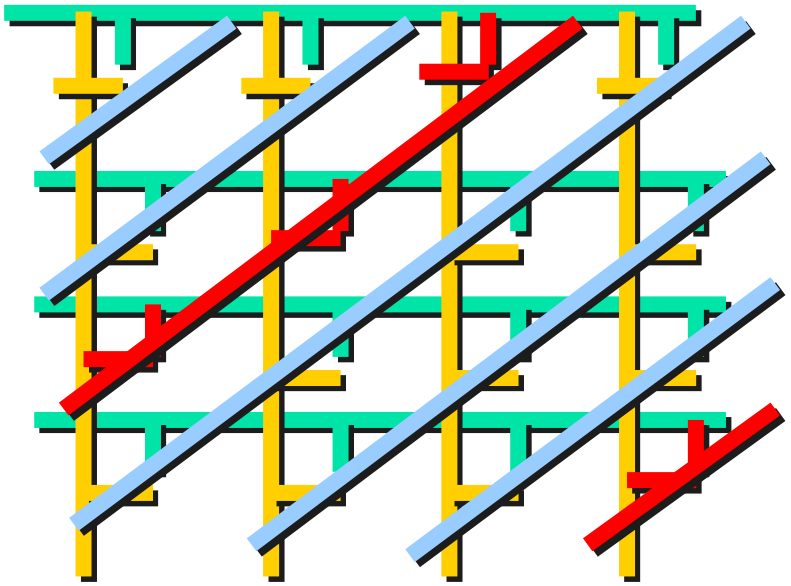

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ARM2 low-cost multiplication hardware: 32-bit result multiply and multiply-accumulate instructions

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Low-cost multiplier employs the barrel shifter and ALU to generate a 2-bit product in each clock cycle.

Early-termination is used to stop the iterations when there are no more ones in the multiply register.

The multiplier logic implements a modified Booth's algorithm that allows to generate 2-bit sub-products in one step.

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ARM high-speed multiplier

High performance multiplication employs redundant binary representation to avoid the carry-propagate delays associated with adding partial products together.

Intermediate results are held as partial sums and partial carries. These results are added in the main ALU at the end of multiplication.

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Carry - save adders

The simplest carry-save adder has 3 inputs and 2 outputs that accept a partial sum, a partial carry and a partial product, all of the same binary weight.

The output produce a new partial sum and a new partial carry where the carry has twice the weight of the sum.

The internal logic of each simple adder is identical to a conventional full adder, but the interconnection structure is different.

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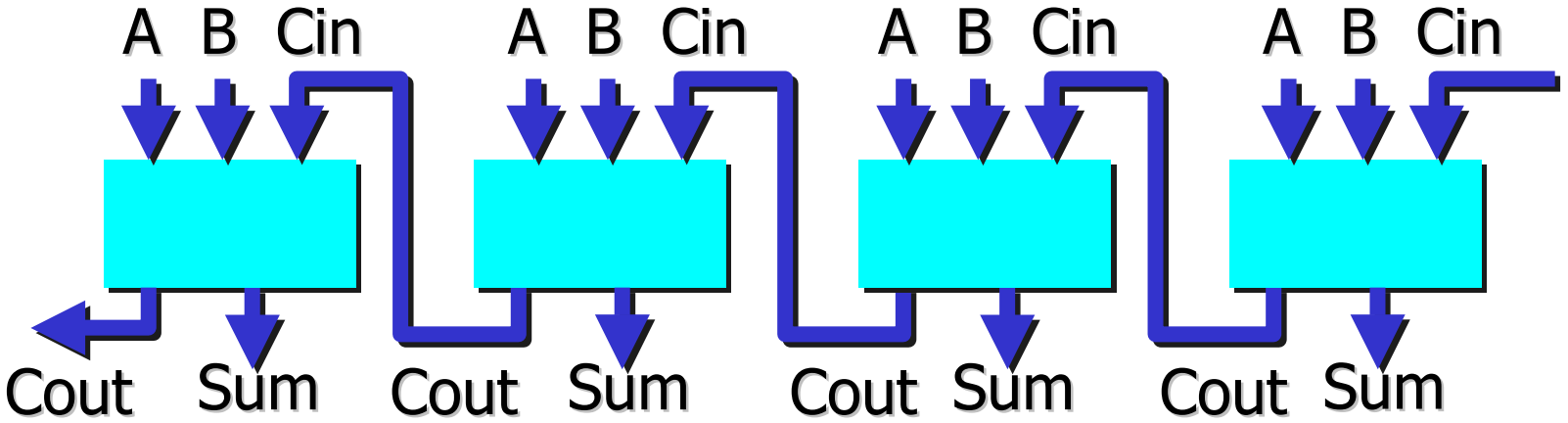
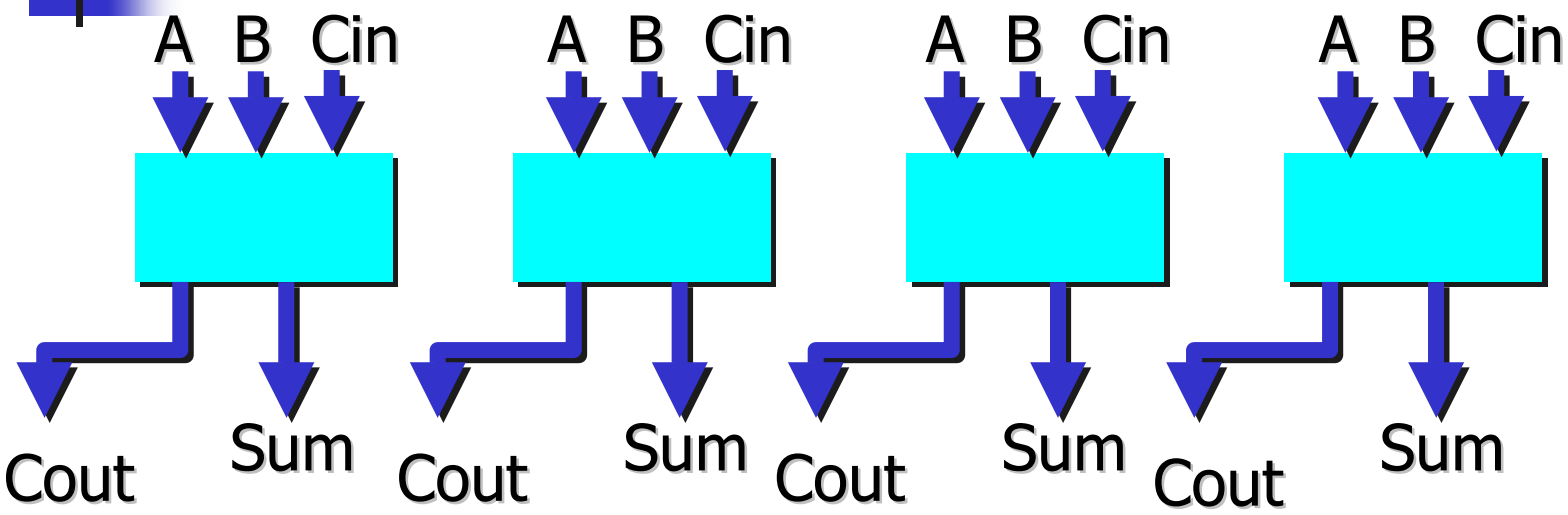
Carry - propagate adder



The carry-propagate adder takes two conventional (irredundant) binary numbers as inputs and produces a binary sum.

Carry - save adder



The carry-save adder takes one binary and one redundant (partial sum and partial carry) input and produces a sum in a redundant binary representation.

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When all partial products have been added, the redundant representation is converted into a conventional binary number by adding the partial sum and partial carry in the carry propagate adder.

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High performance multiplier

High speed multipliers have several layers of carry-save adders, each handling one partial product.

In some ARM cores the carry-save array has four layers of adders, each handling two multiplier bits (see Booth algorithm), so the array can multiply eight bits per clock cycle.

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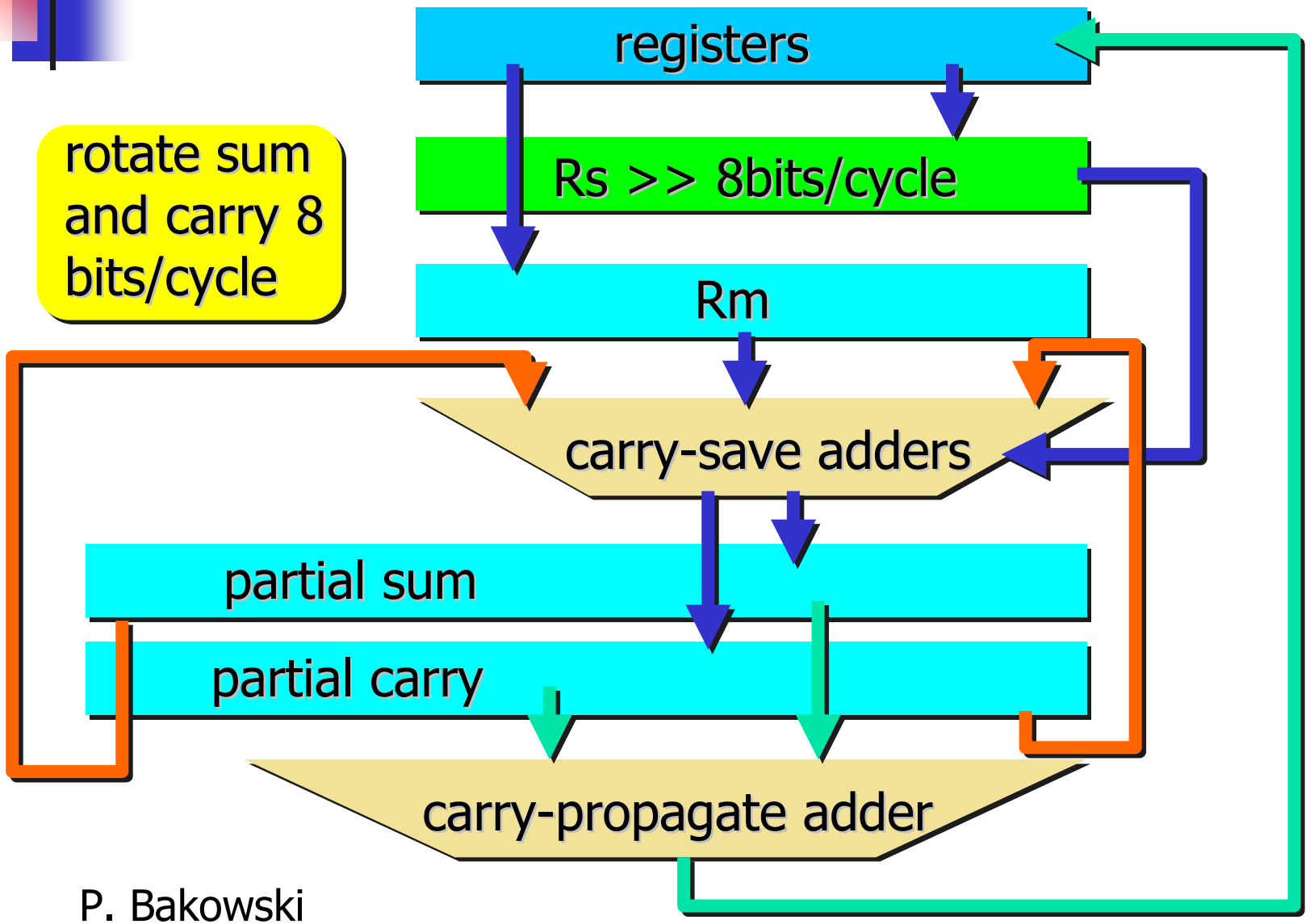
High speed multiplier organization

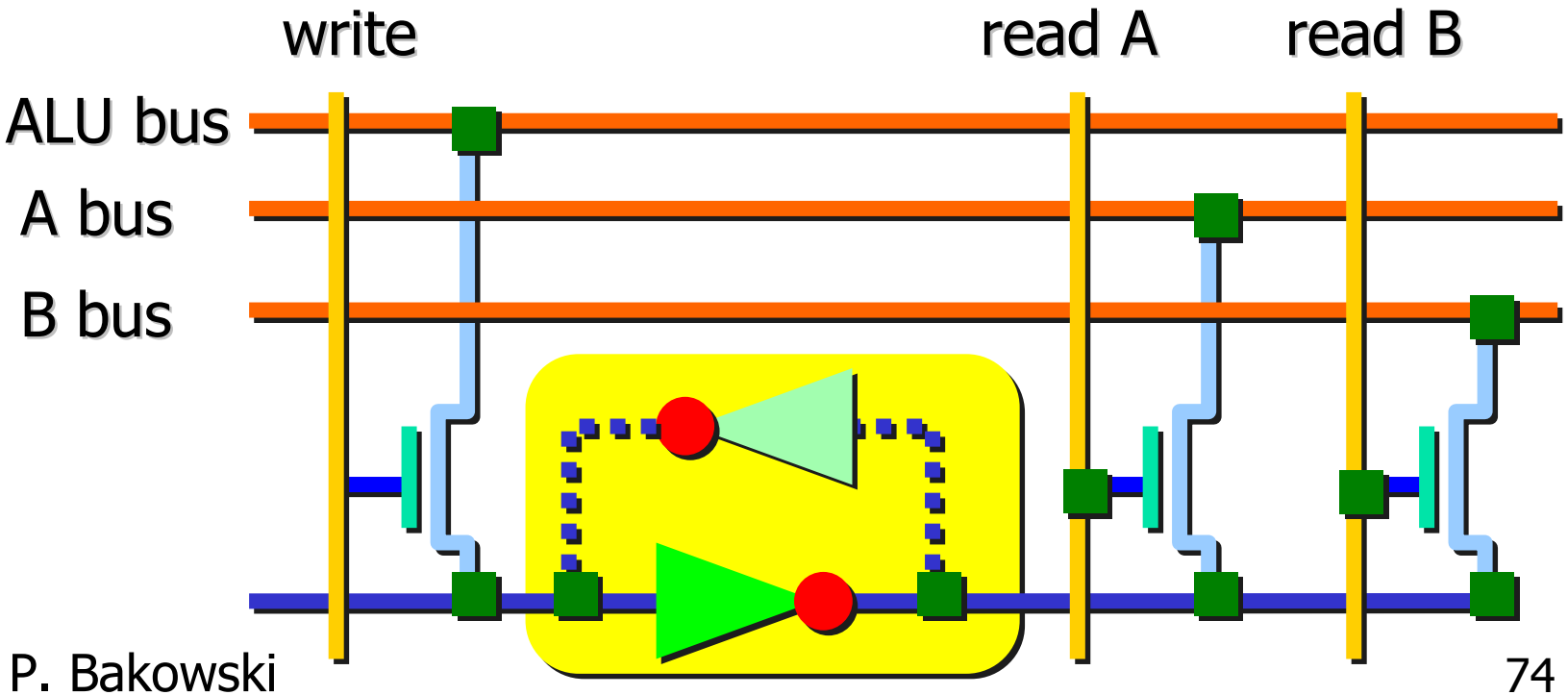


ARM register bank

ARM has 31 general-purpose 32-bit registers containing almost 1 Kbytes of data.

ARM register cell

The transistor circuit of the register cell used in ARM cores up to the ARM6 is based on an asymmetric cross-coupled pair of CMOS inverters which is overdriven by a strong signal from the ALU bus when the register contents are changed.



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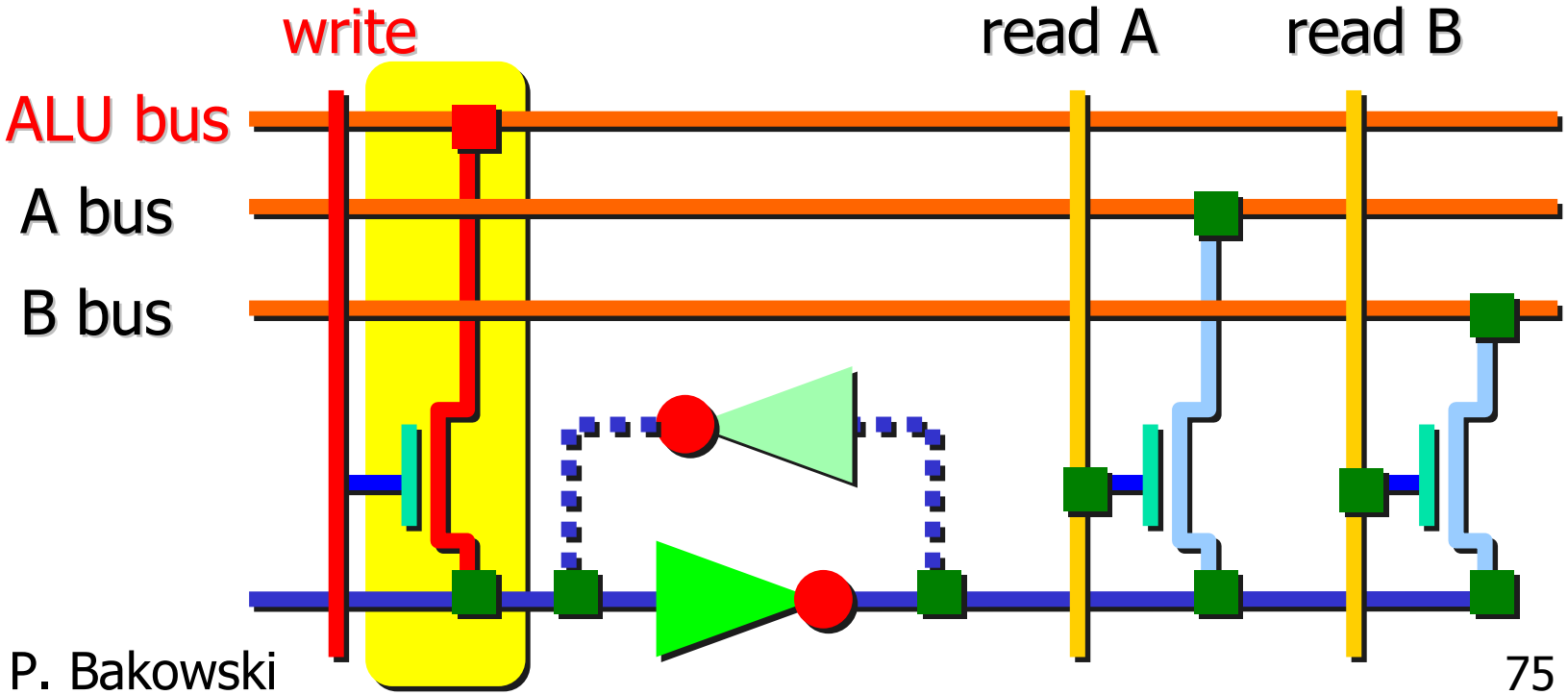
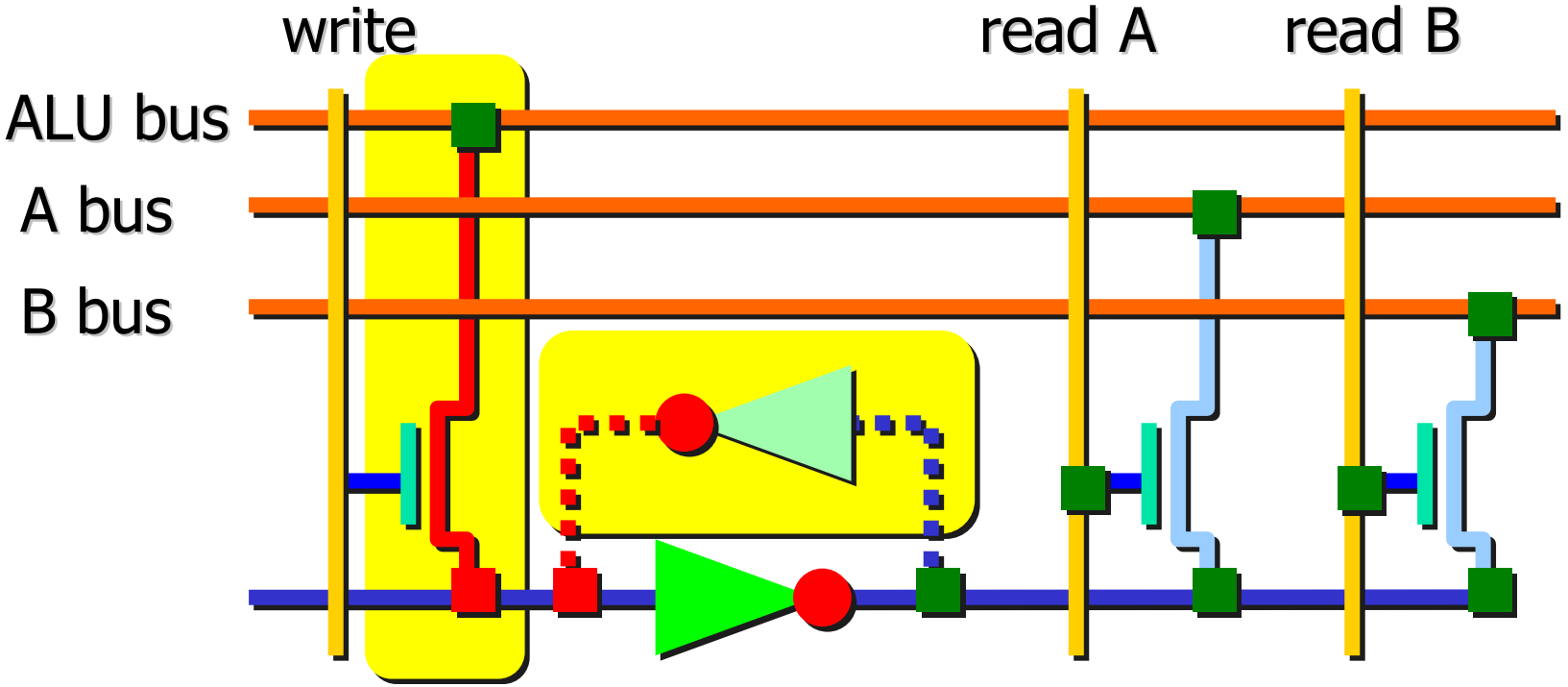


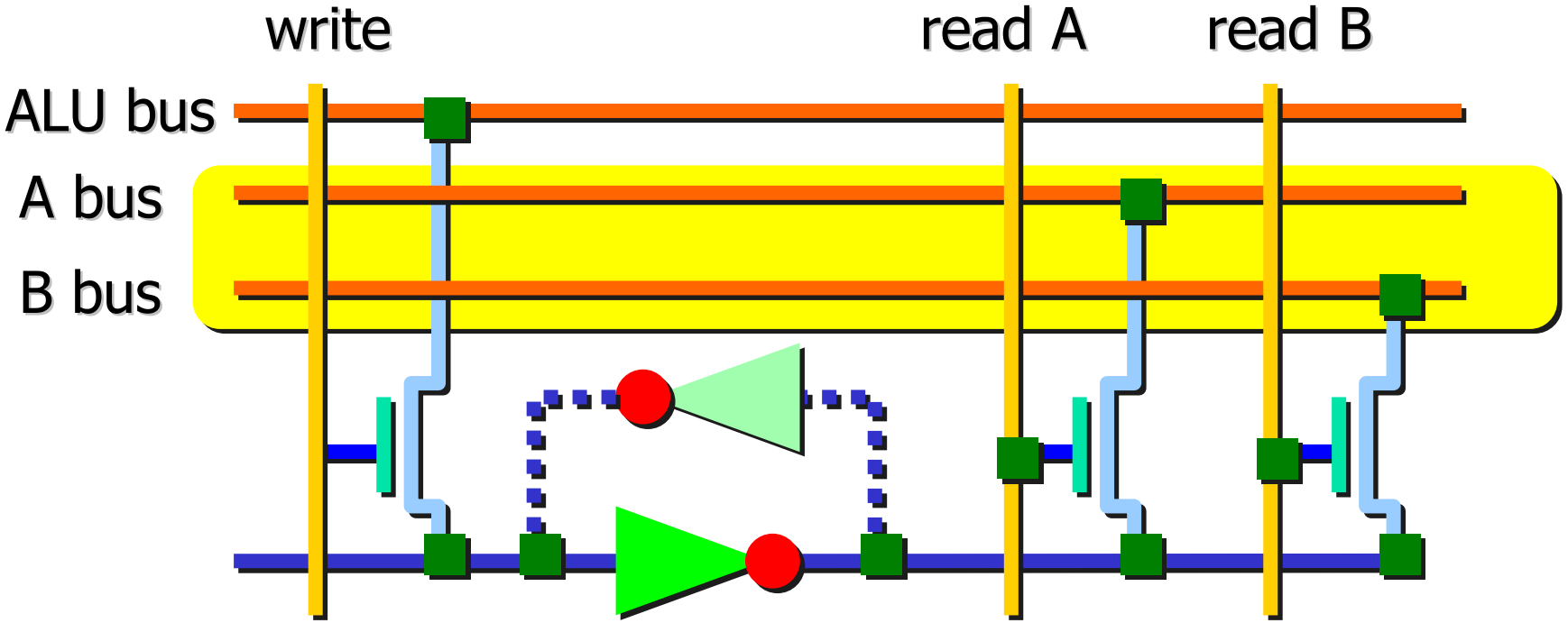
ARM register cell

The feedback inverter is made weak in order to minimize the cell's resistance to the new value.



ARM register cell

The A and B buses are pre-charged to Vdd during phase 2 of the clock cycle, so the register cell needs only discharge the read buses, which it does through n-type pass transistors when the read lines are enabled.



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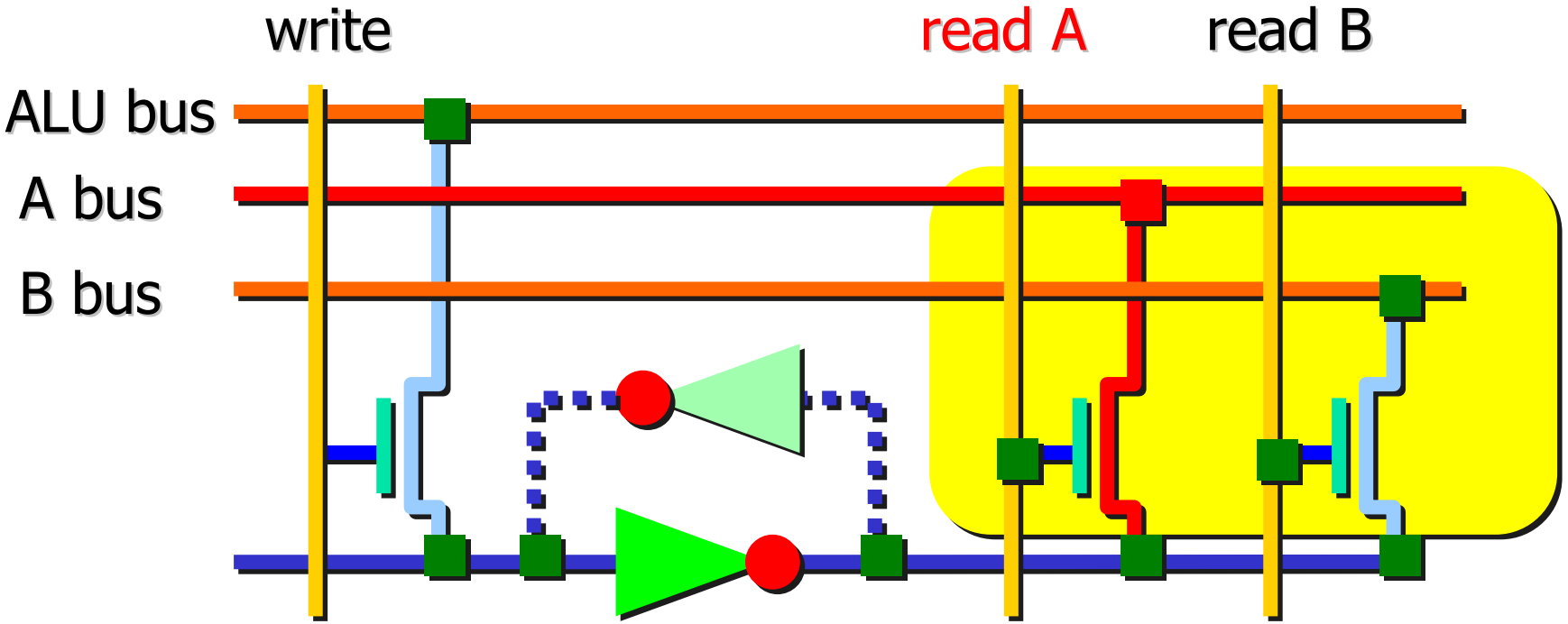
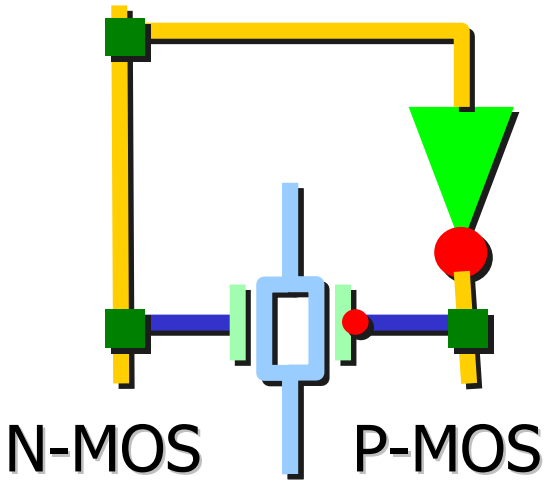


ARM register cell

This register cell works well with a 5 V supply.

In new designs ARM uses lower supply voltages where writing a '1' through the n-type pass transistor would be impossible.

Instead it uses a full CMOS transmission gate requiring complementary write enable control lines.



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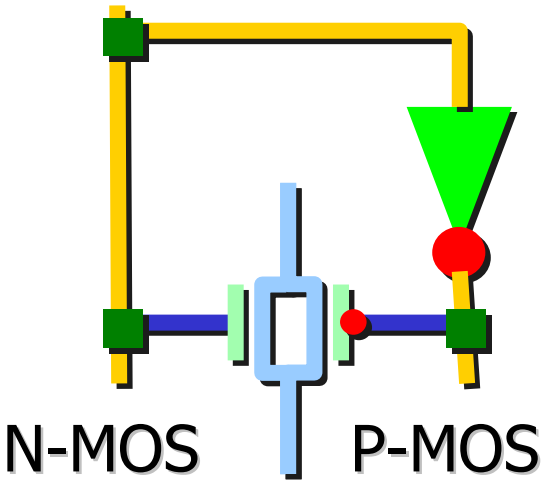

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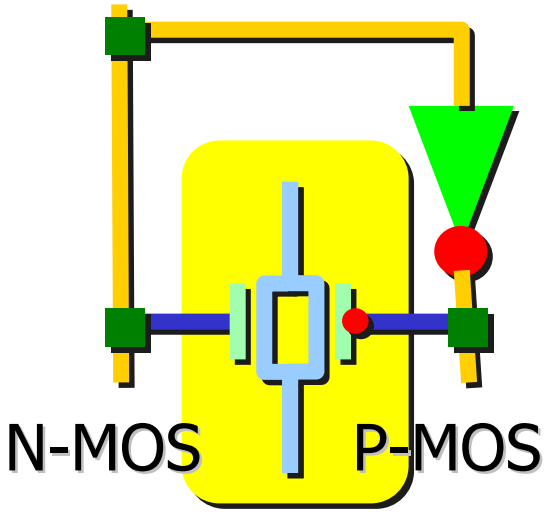

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The register cells are arranged in columns to form a 32-bit register, and the columns are packed together to form the complete register bank.

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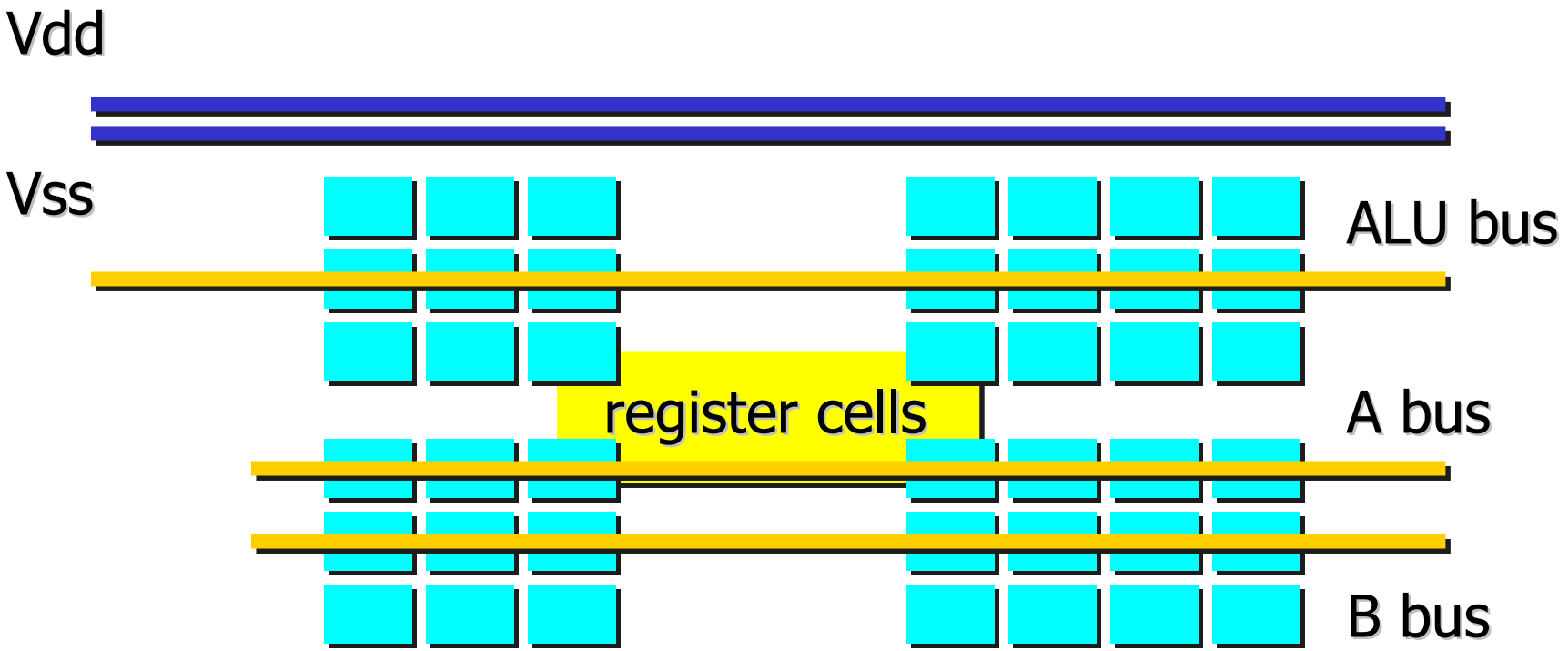

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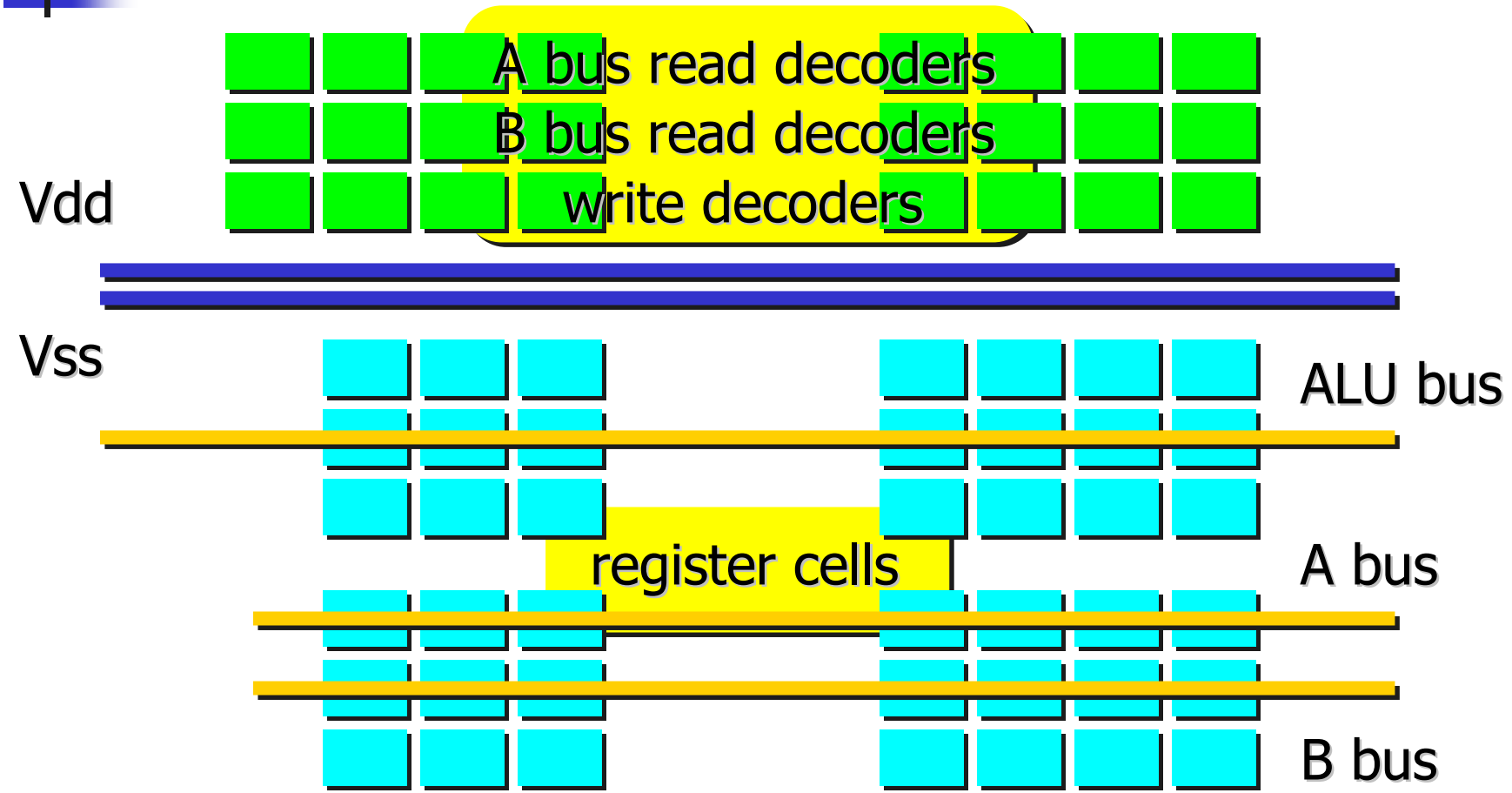

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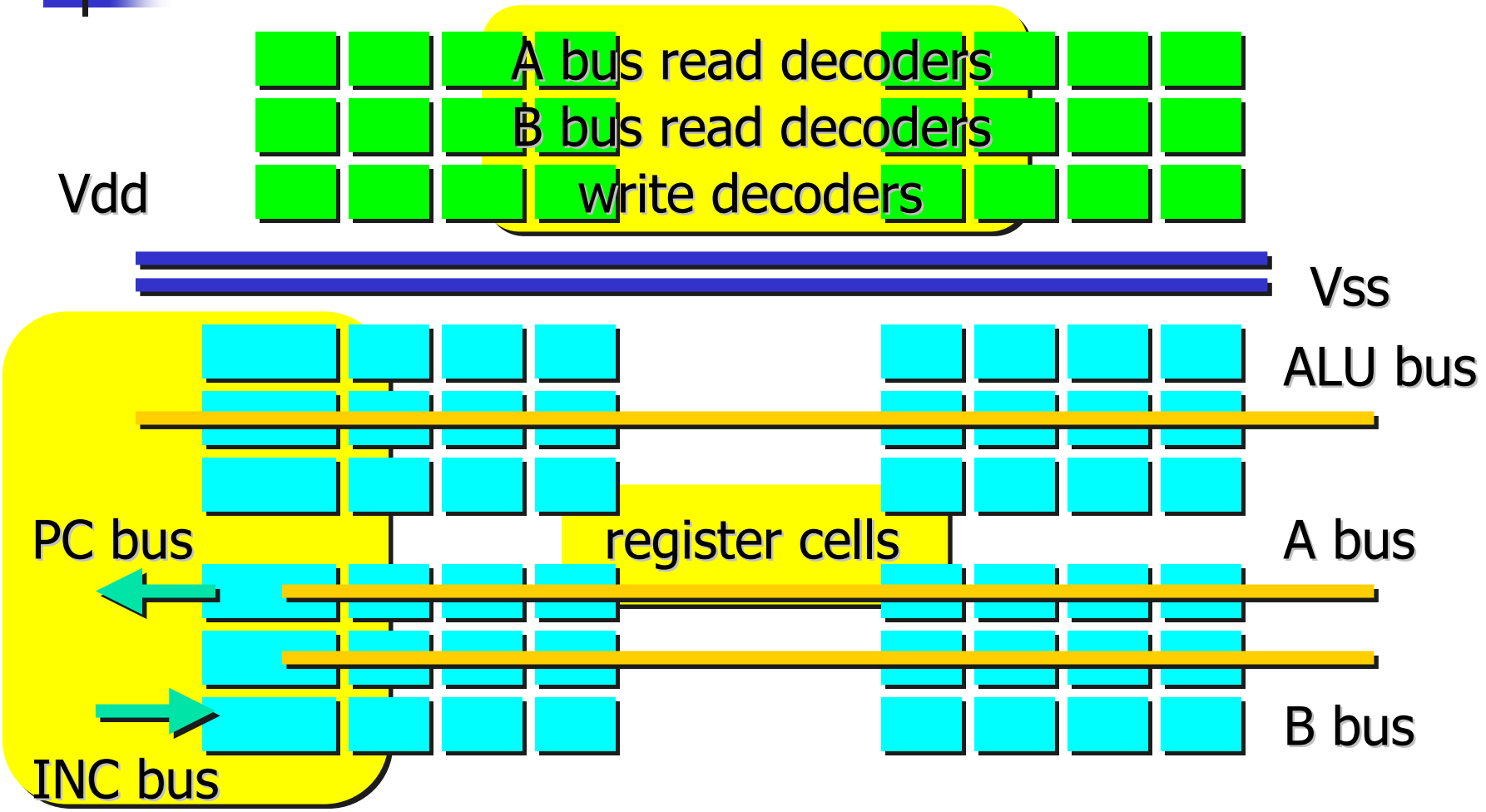

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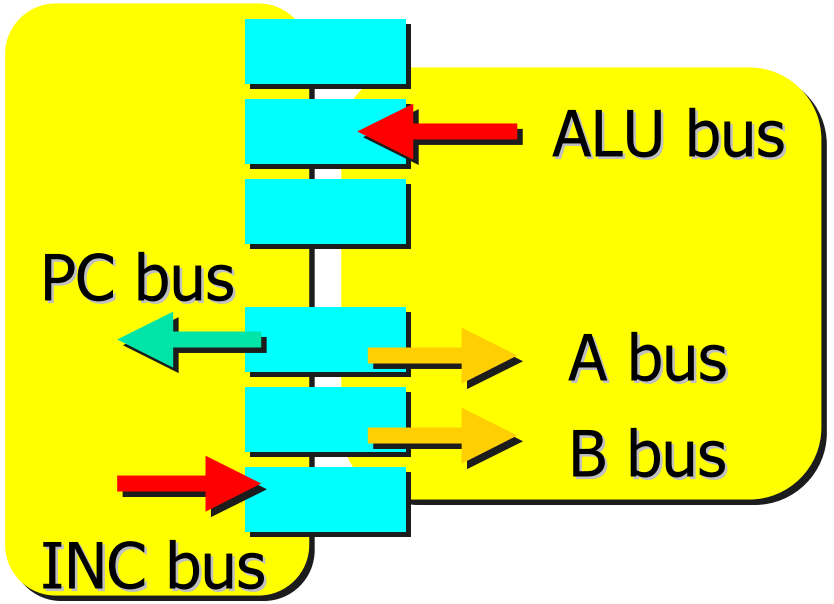

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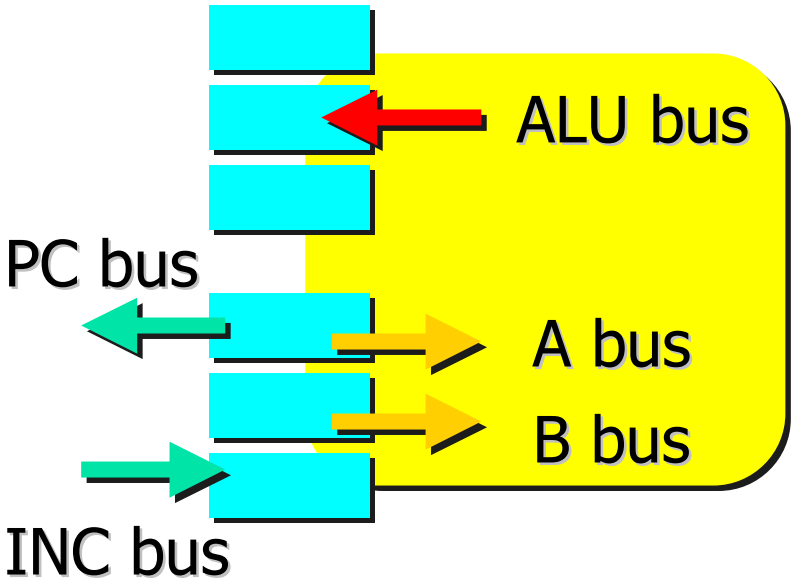

ARM data path layout

The ARM datapath is laid out to a constant pitch per bit.

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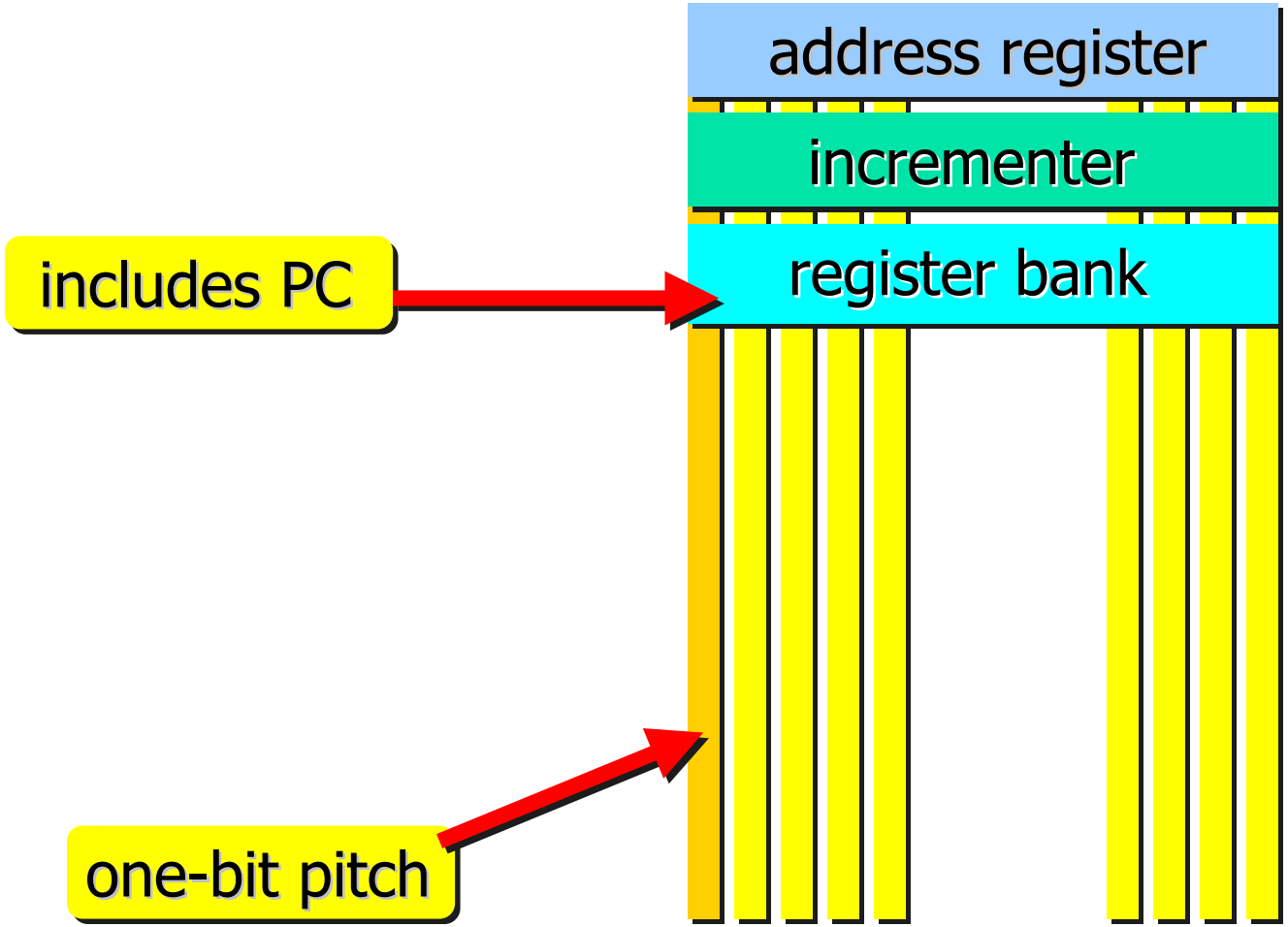

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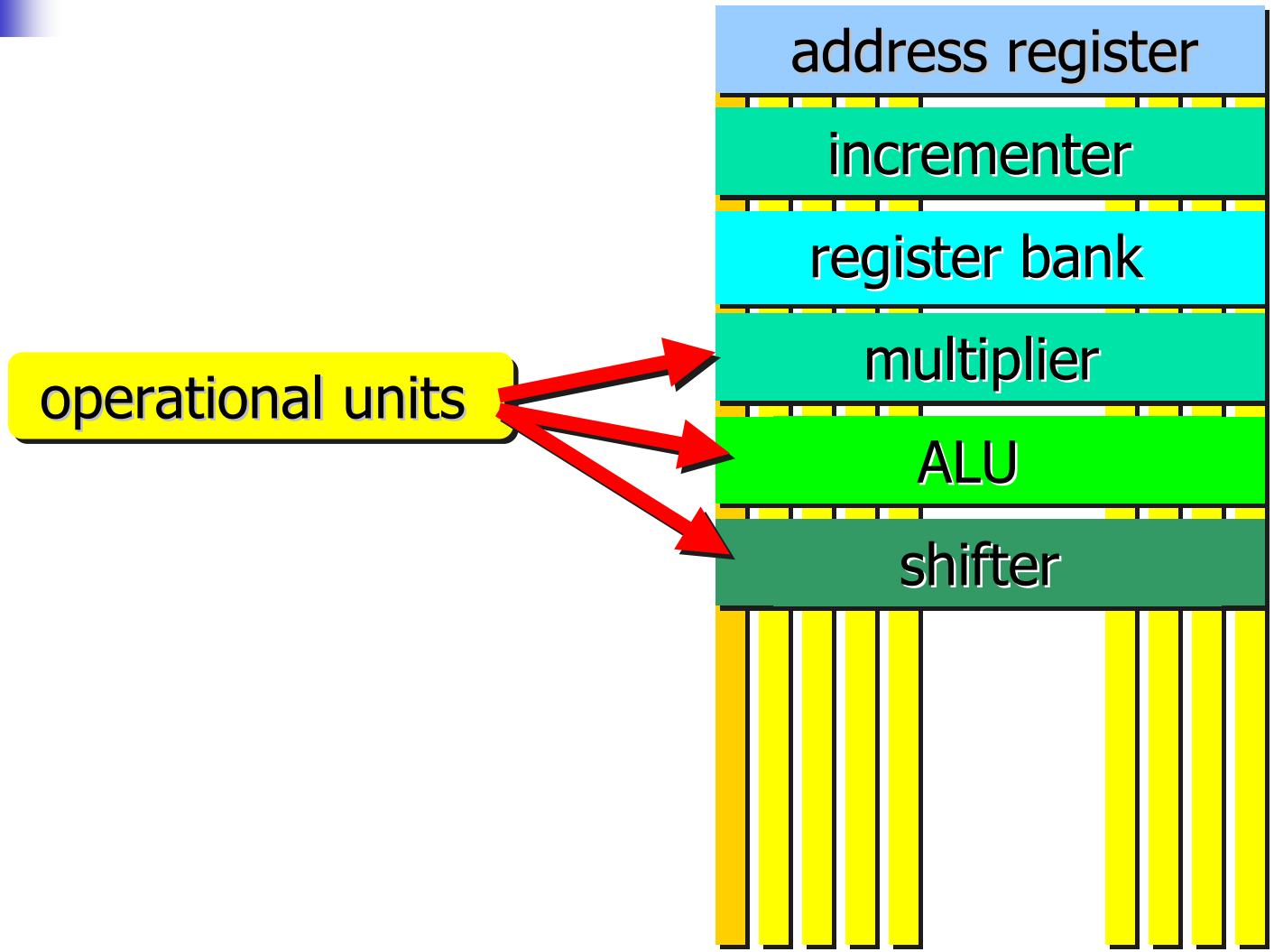

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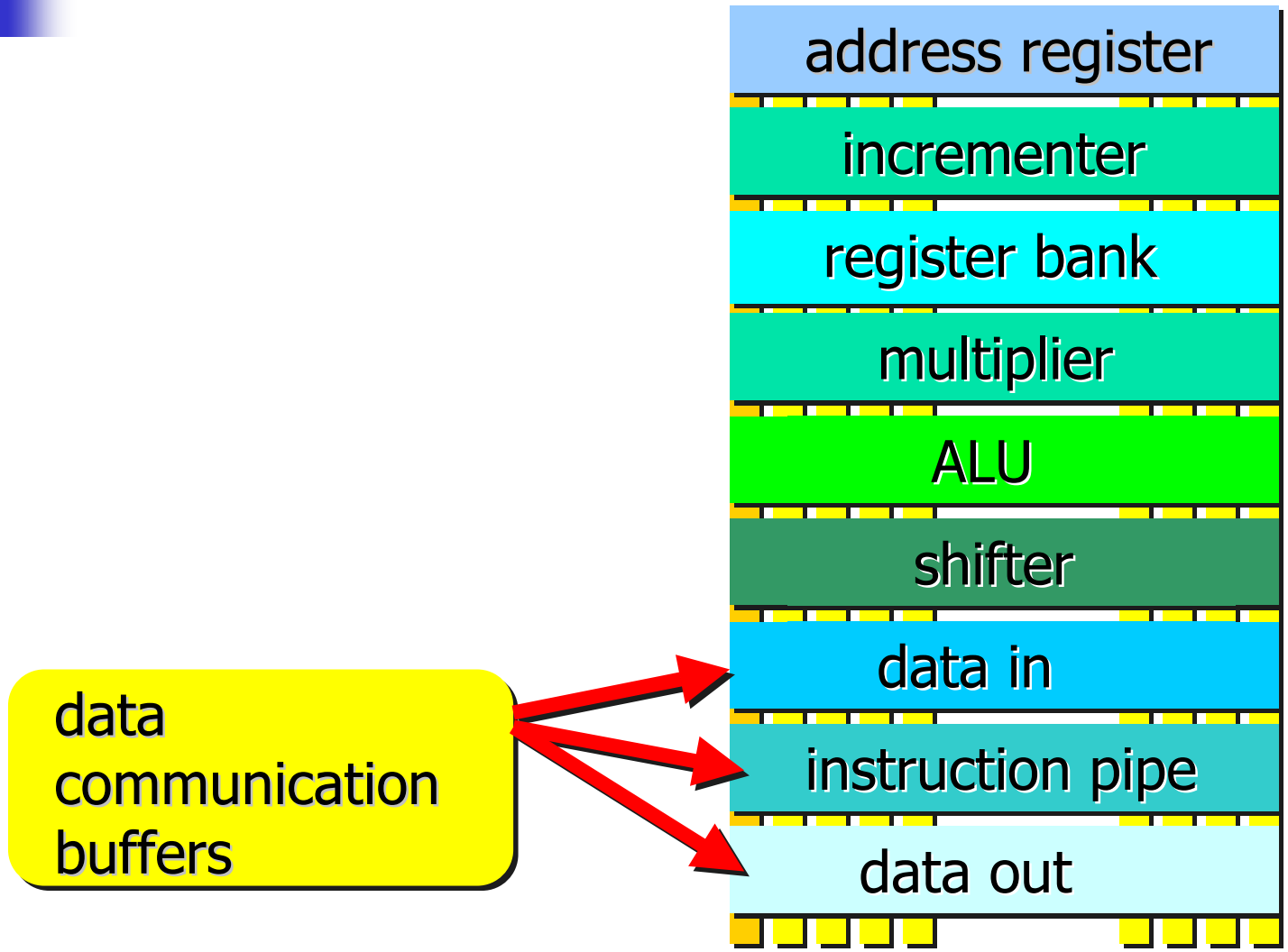

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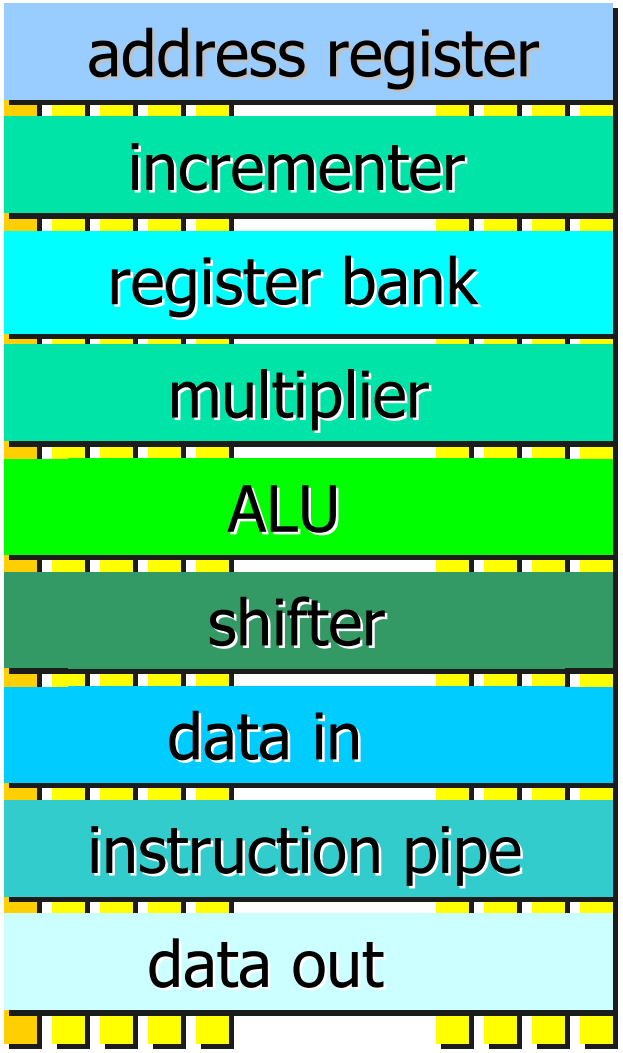

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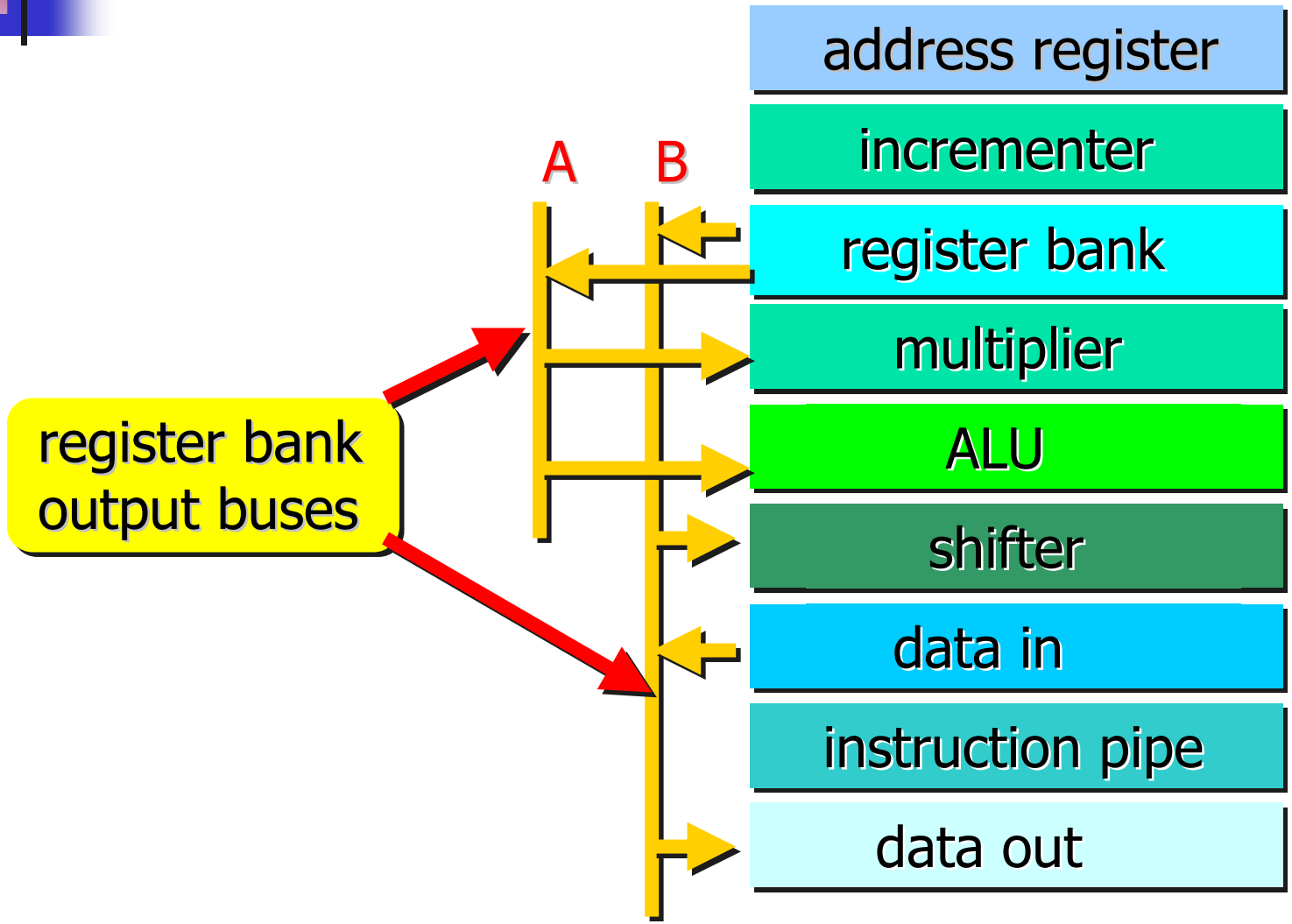

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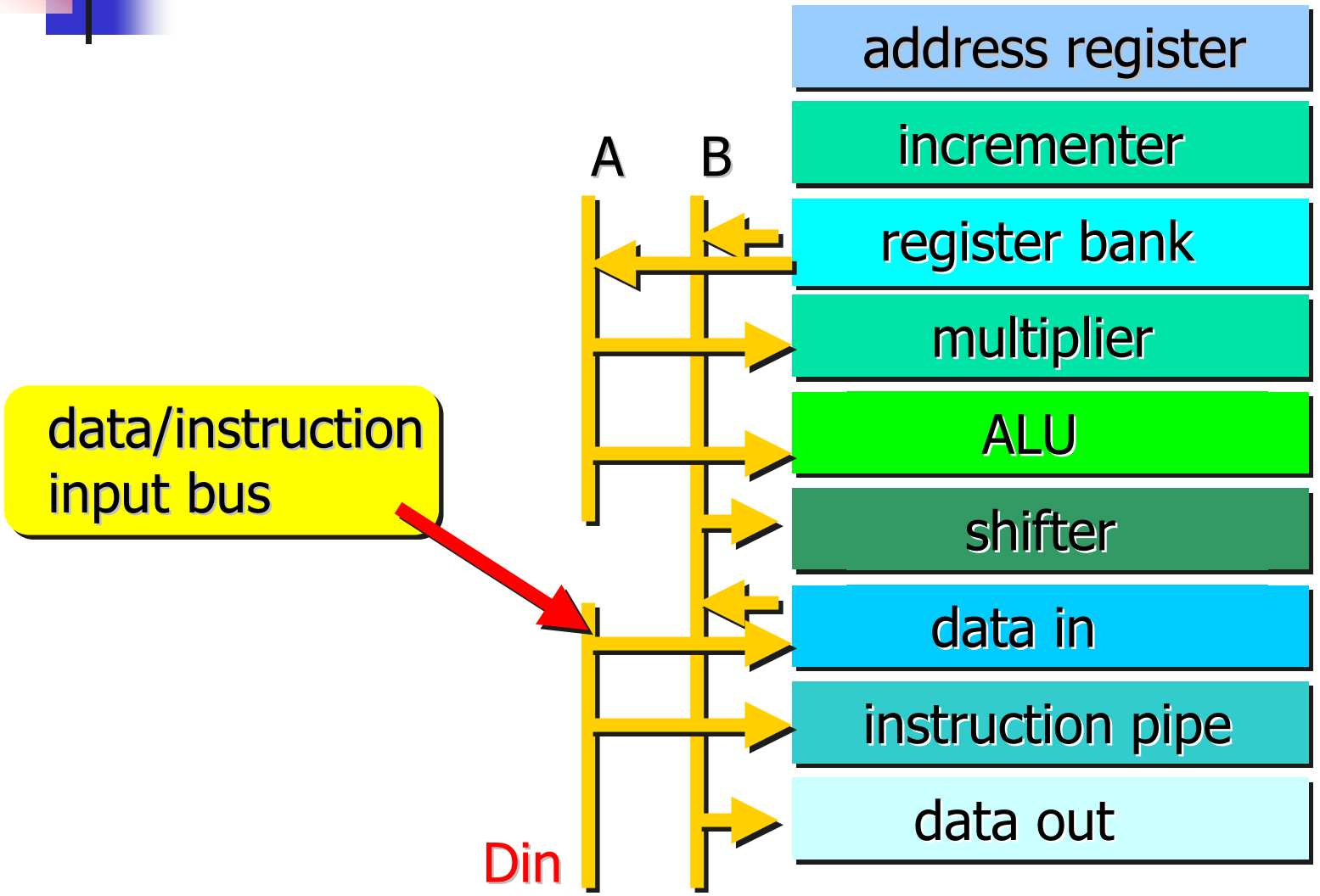

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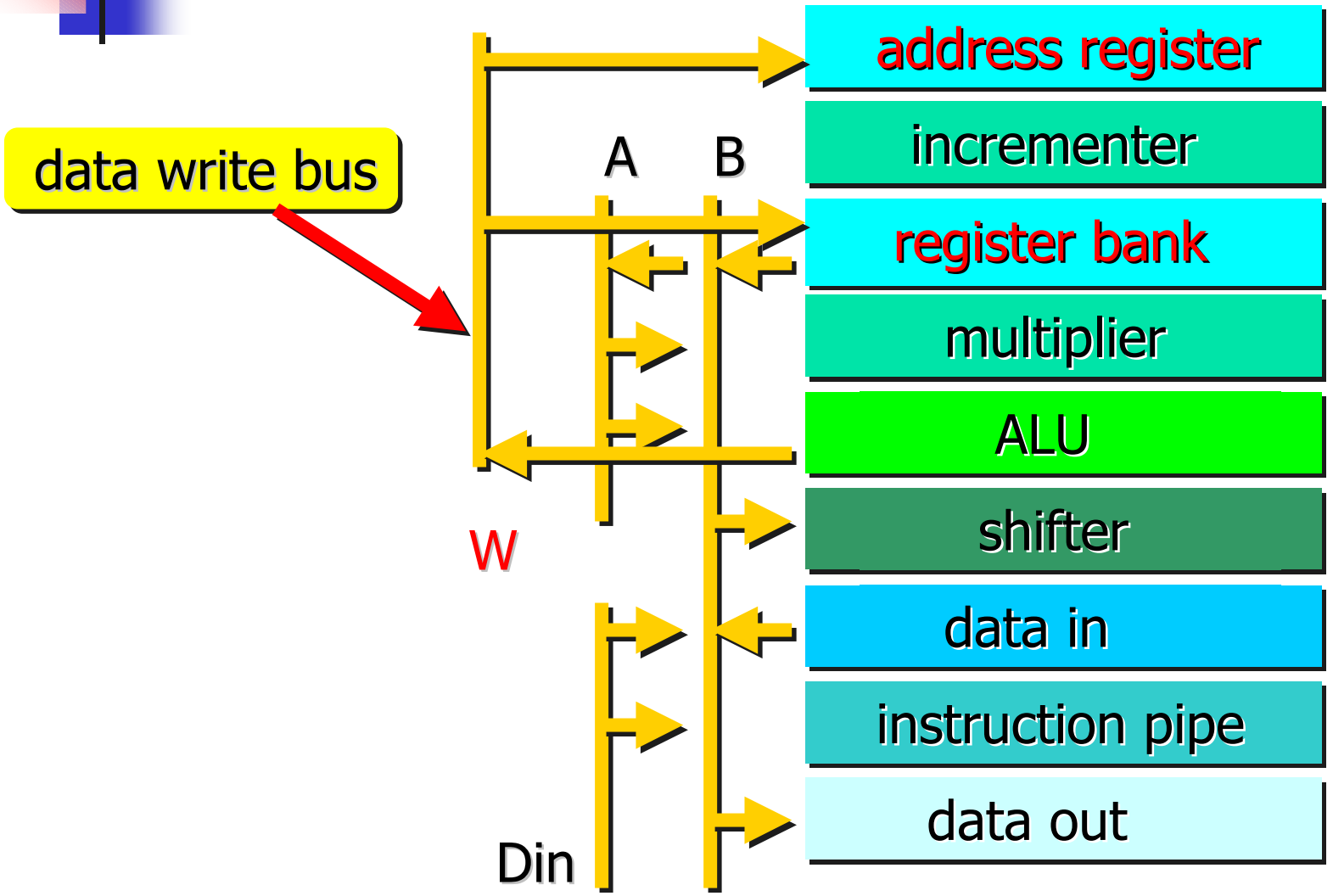

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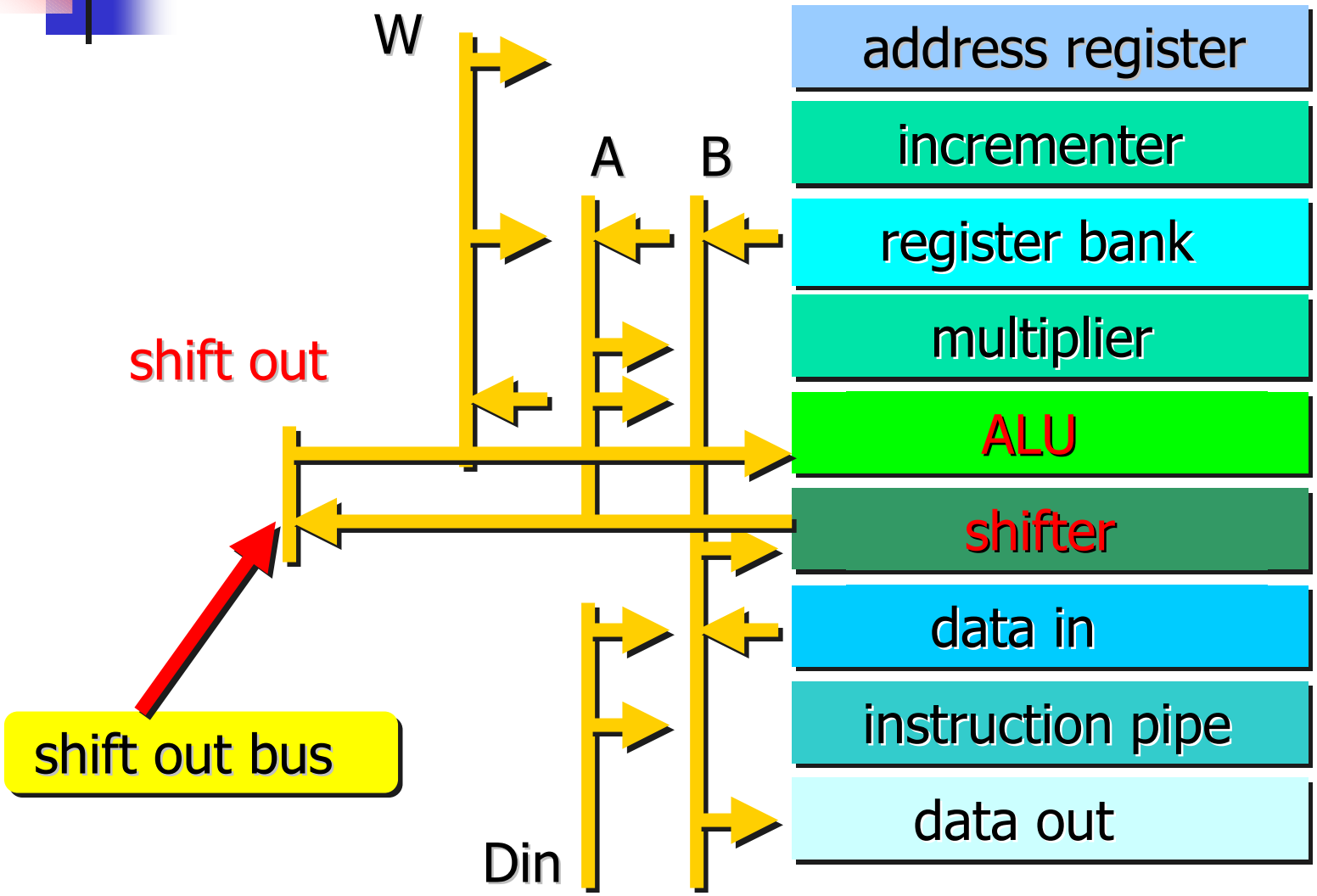

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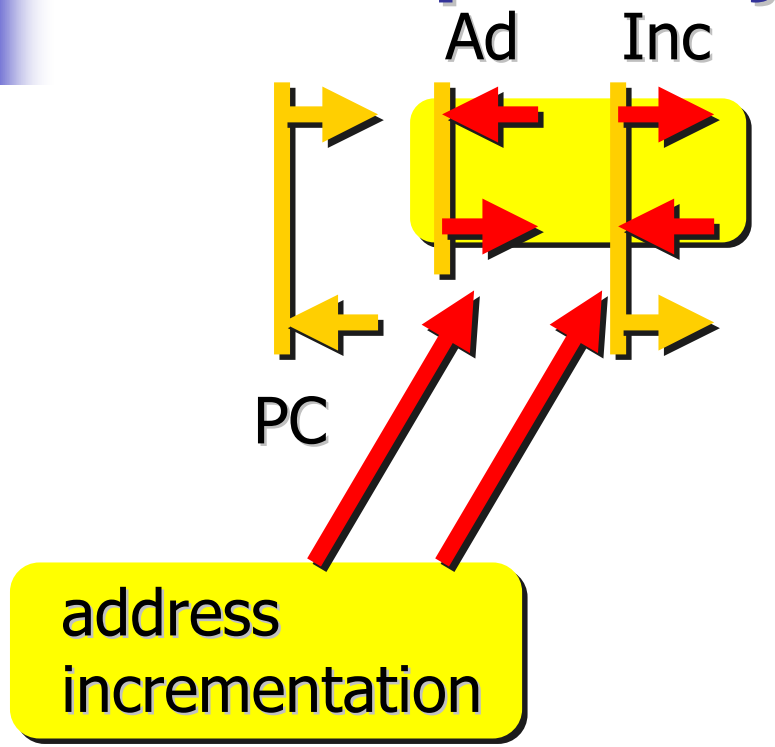

address register

incrementer

register bank

multiplier

ALU

shifter

data in

instruction pipe

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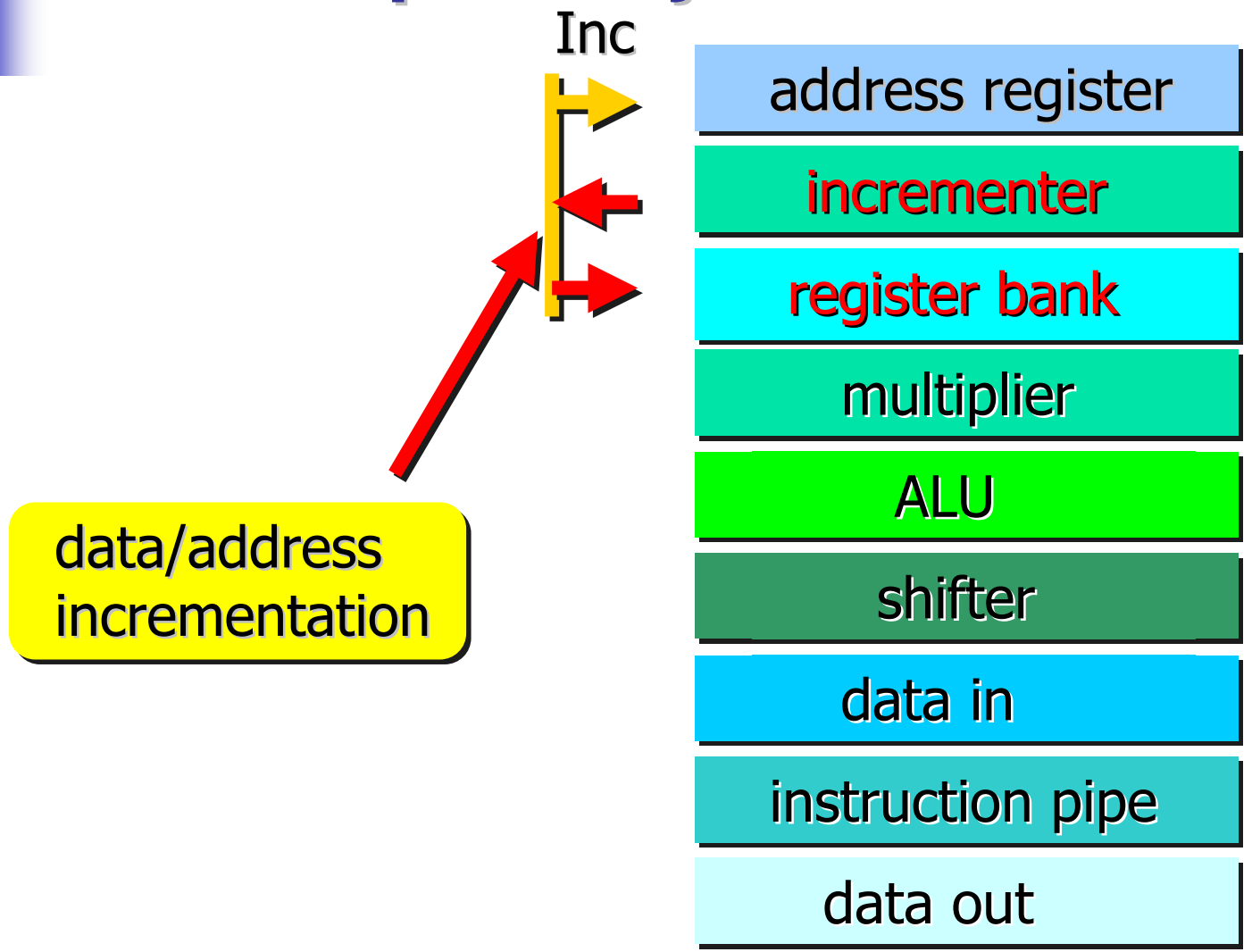

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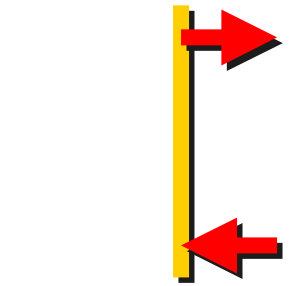

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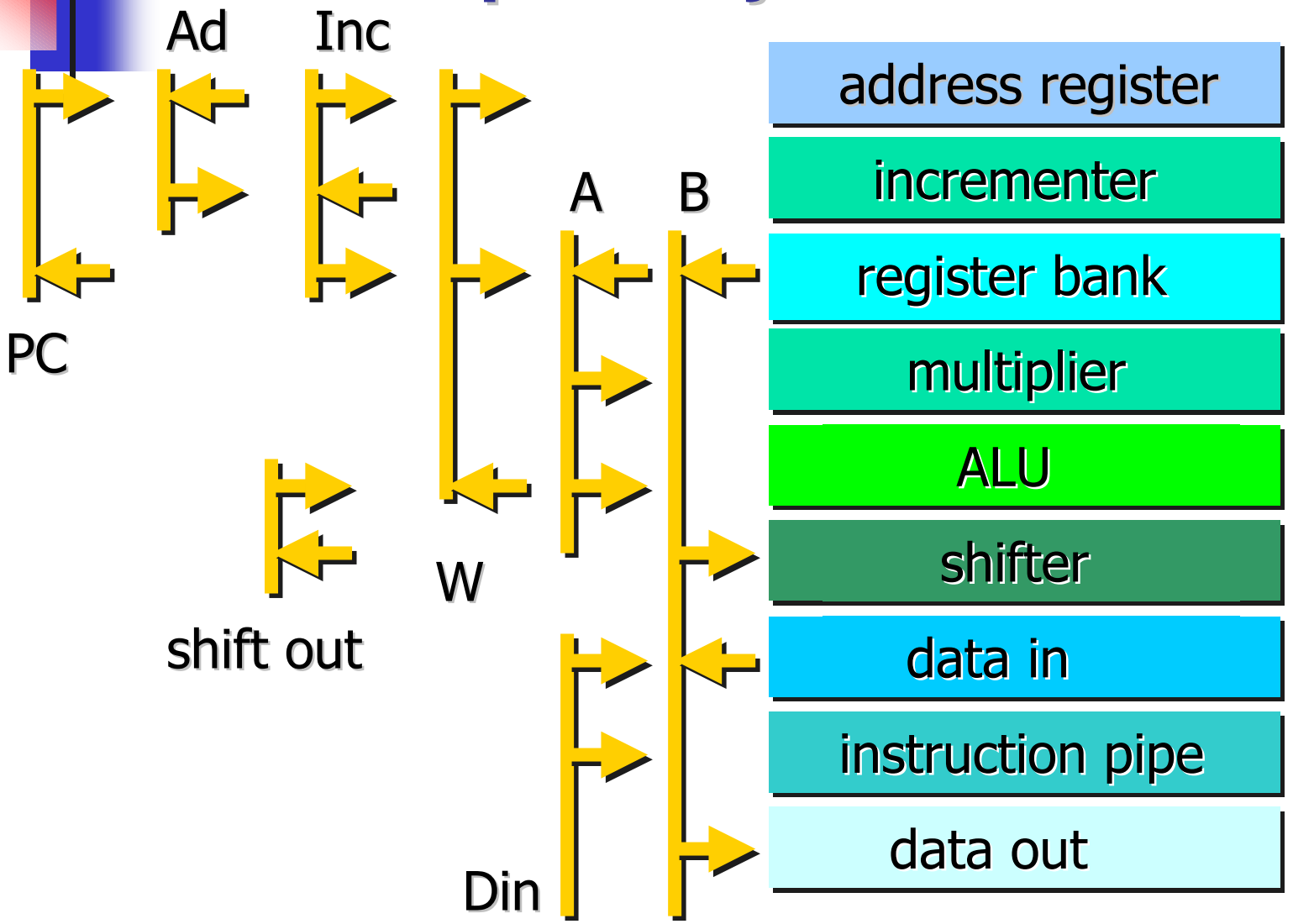

ARM control path

The control path in simpler ARM cores has three structural components:

- an instruction decoder PLA
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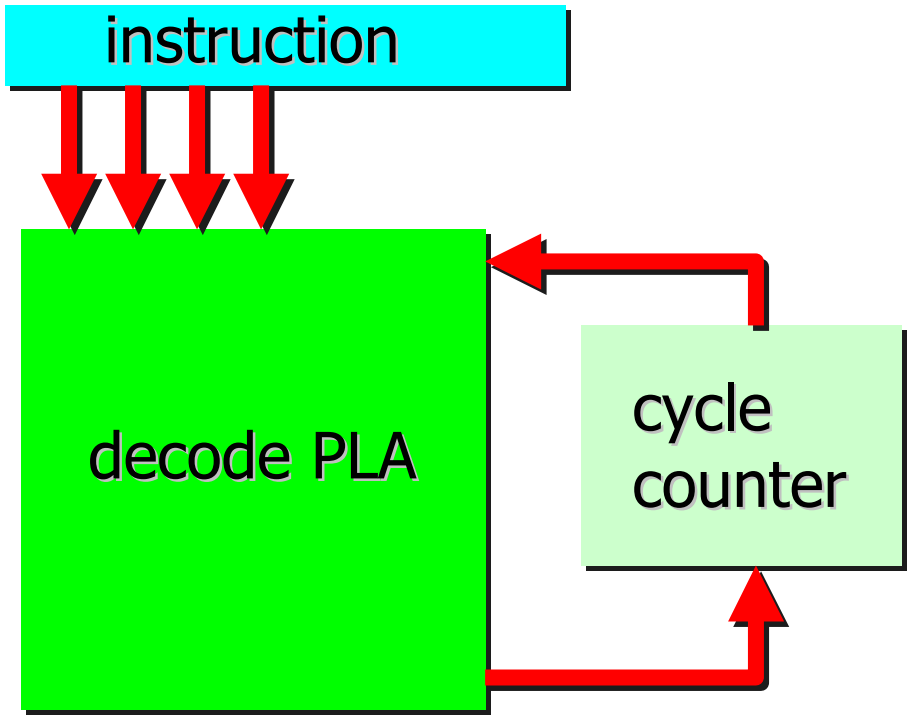
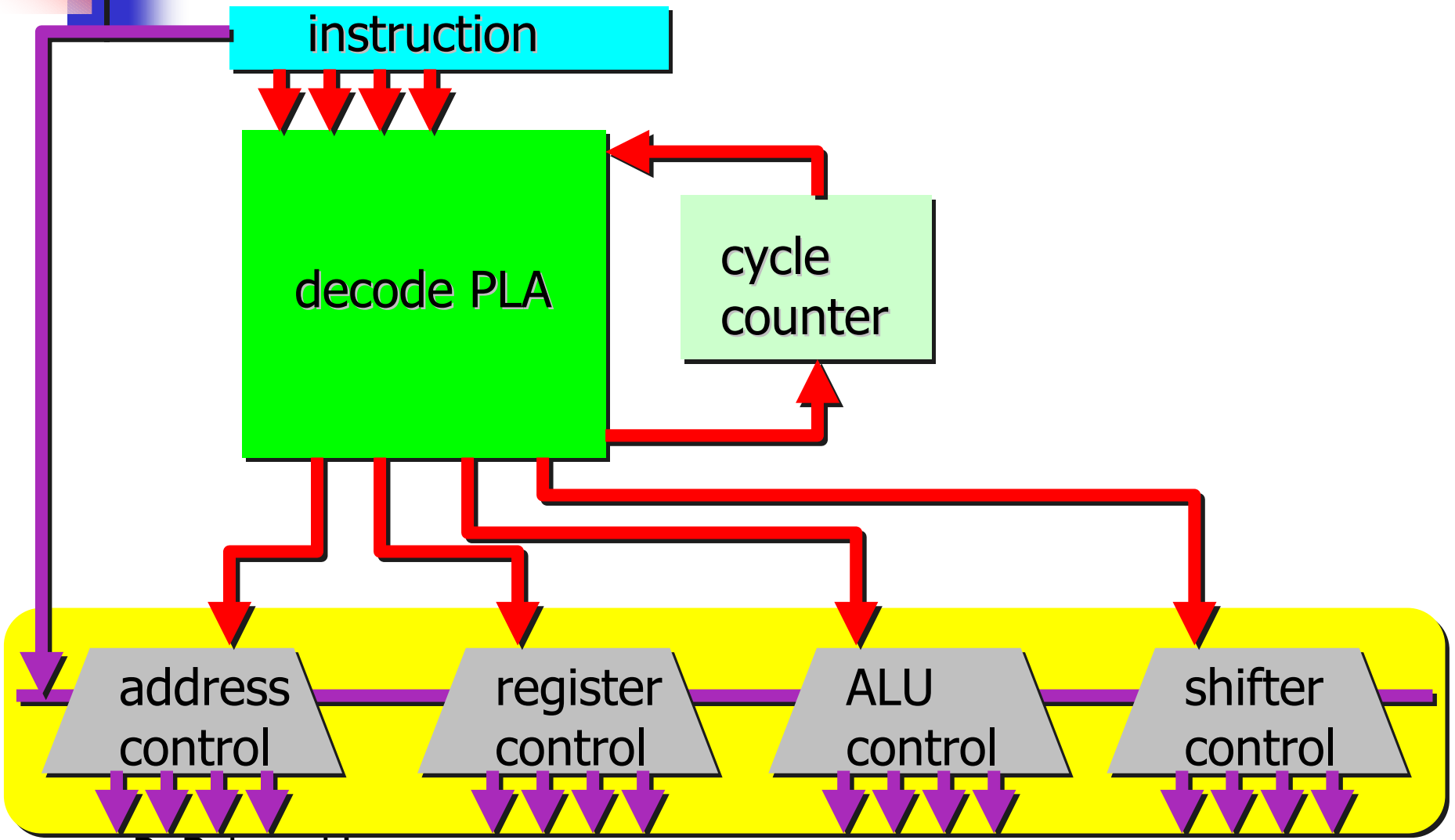
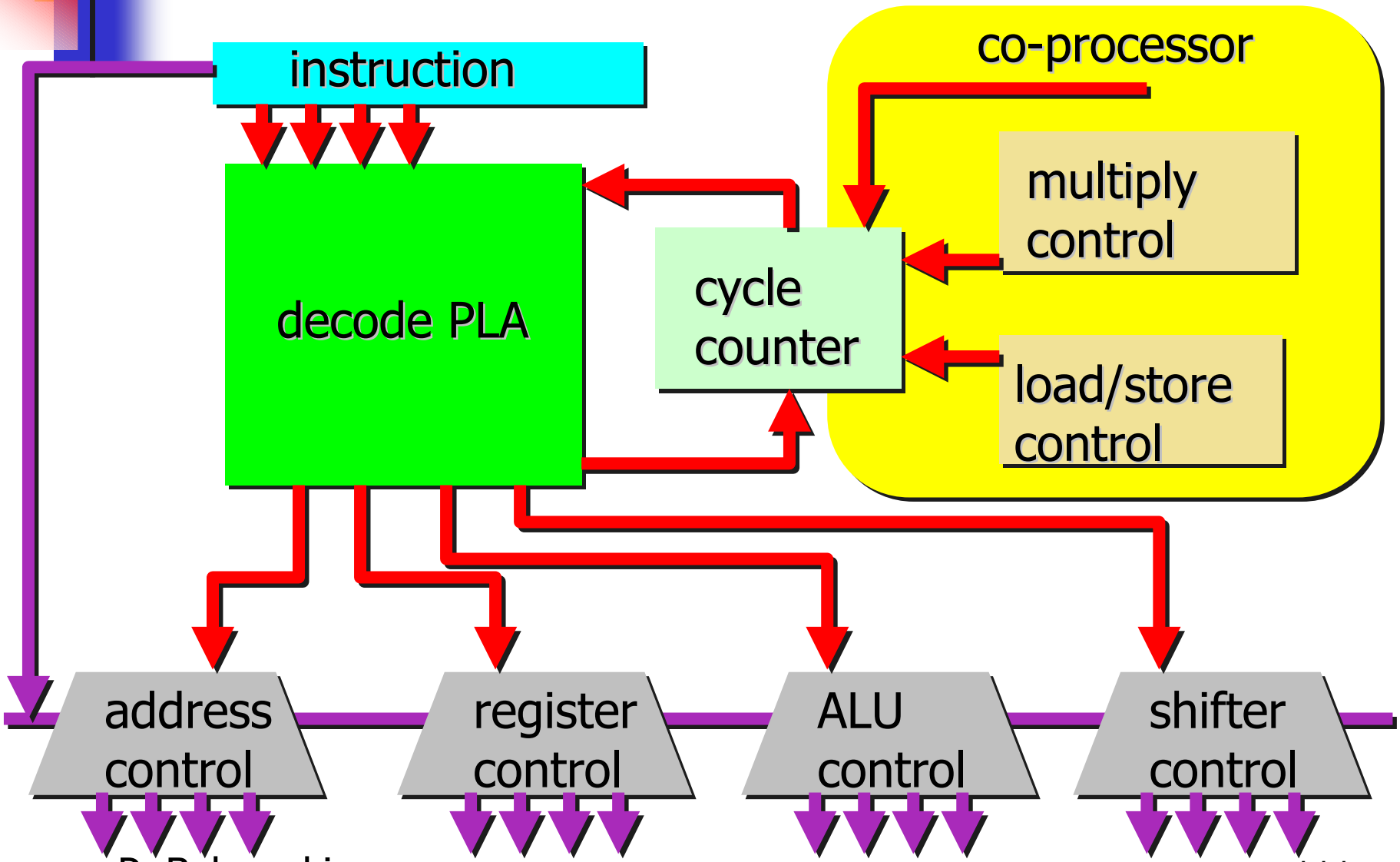


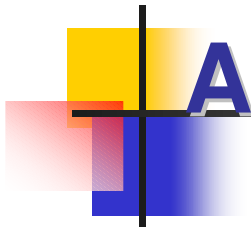
Class of instruction: ALU, load/store, branch, co-processor,..

ARM secondary control



ARM decentralized control





ARM hard cores versus soft cores

There are two kinds of supports for the implementation of ARM cores:

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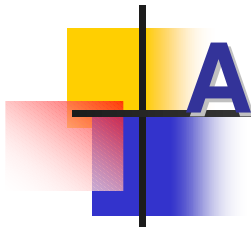

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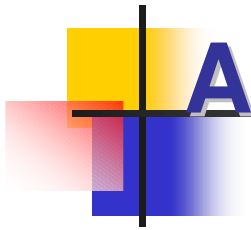

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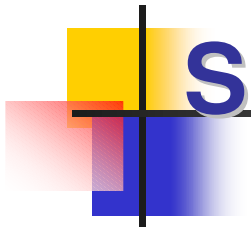

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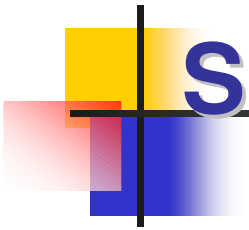

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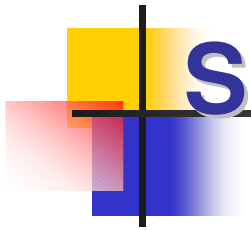

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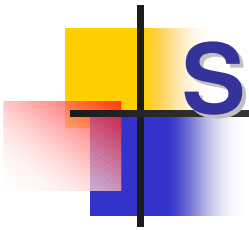

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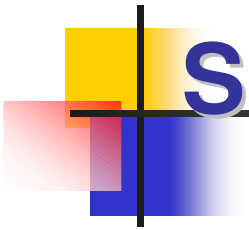

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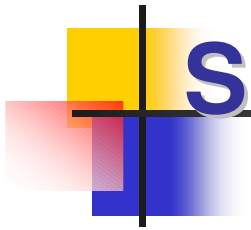

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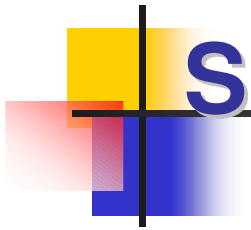

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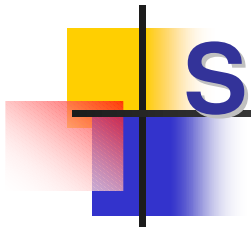

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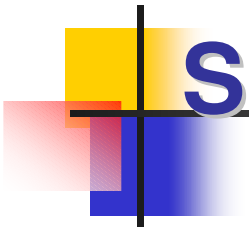

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