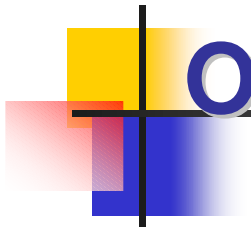
The ARM Architecture

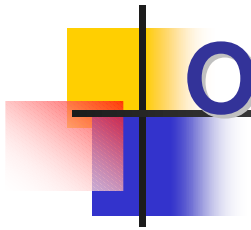
P. Bakowski

bako@ieee.org



Outline

- ARM history
- ARM architecture
- ARM ISA features
- ISA extensions
- Architecture implementations



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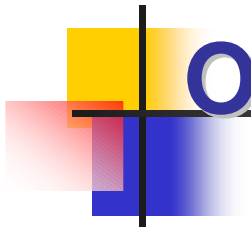

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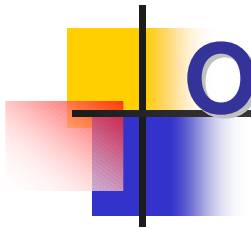

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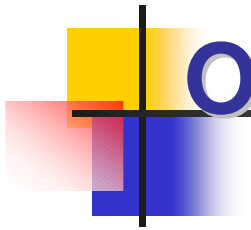

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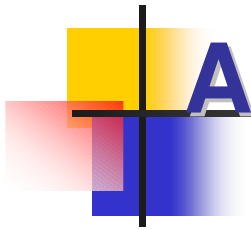

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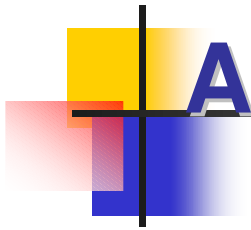

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  - ARMv2 – 32-bit data; 26-bit address

    simple RISC architecture, 30 K transistors, no microcode, no cache

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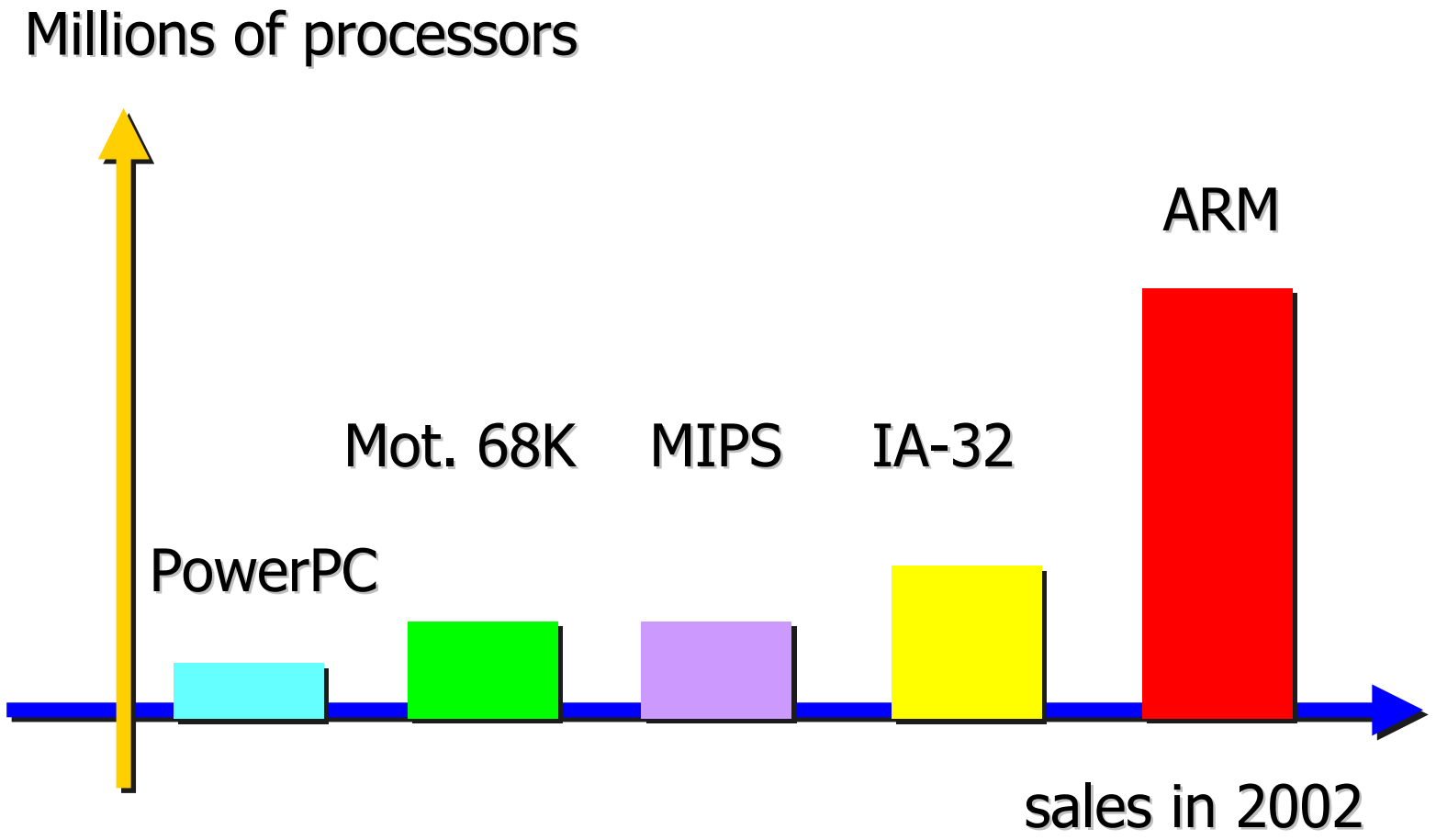
ARM place in the market

ARM is leading provider of 32-bit embedded RISC microprocessors:

- common architecture: compatible versions
- high performance
- low power consumption
- low system cost

ARM place on the market of µP



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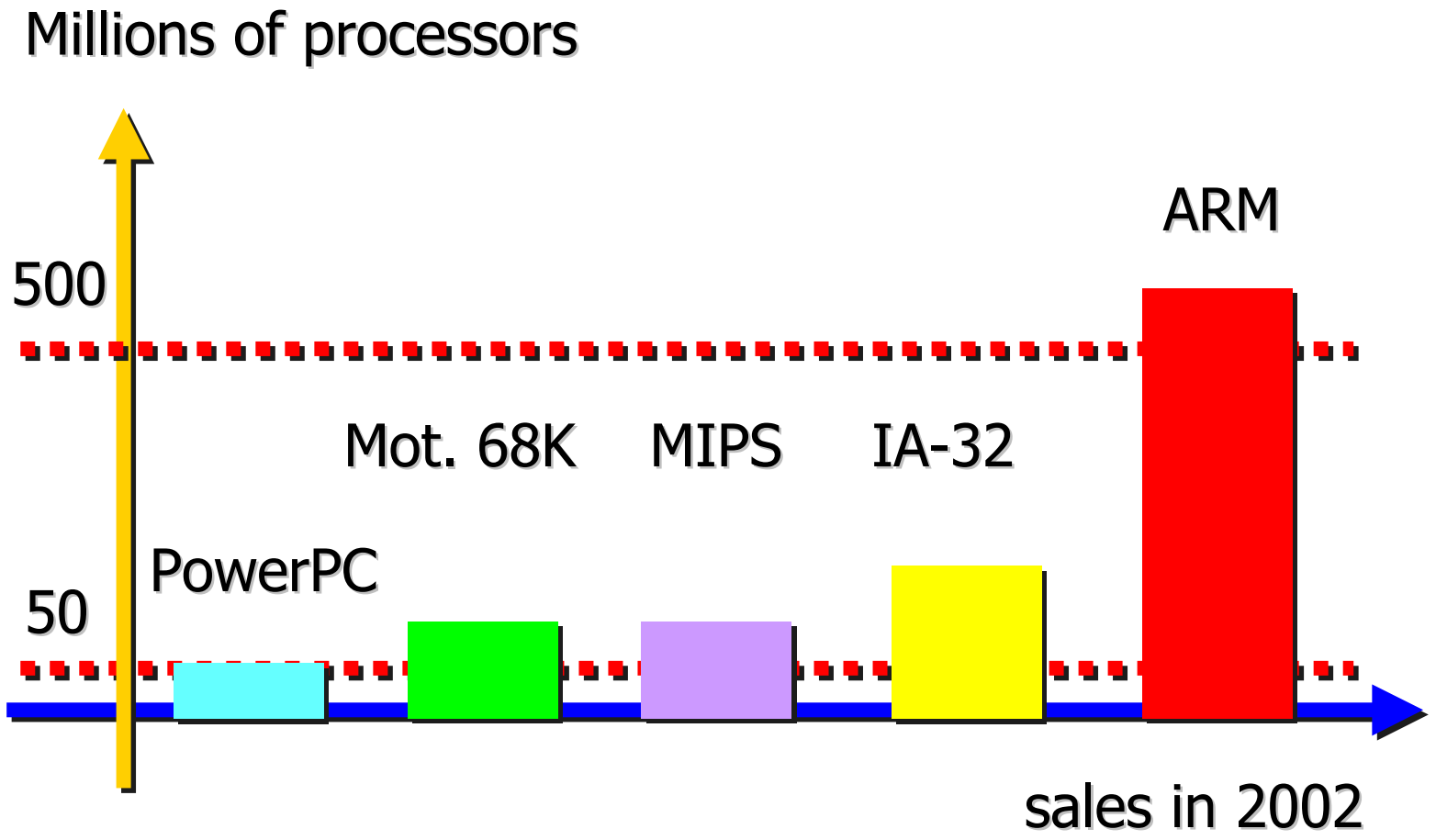

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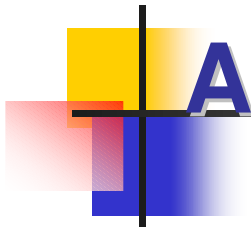
Embedded real-time systems for:

- Mass storage
- Automotive
- Industrial
- Network

- Secure applications – smartcards and SIMs
- Open platforms running complex OS



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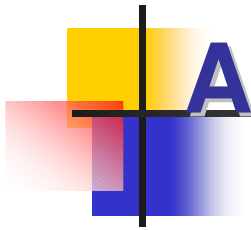

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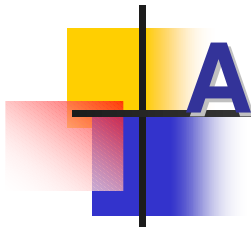

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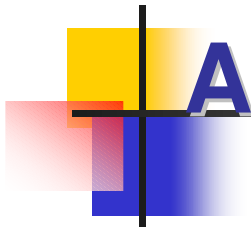

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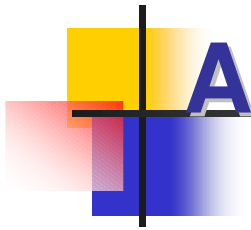

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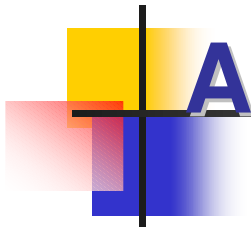

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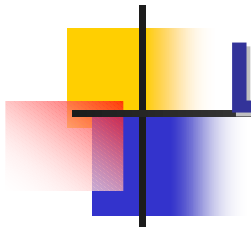

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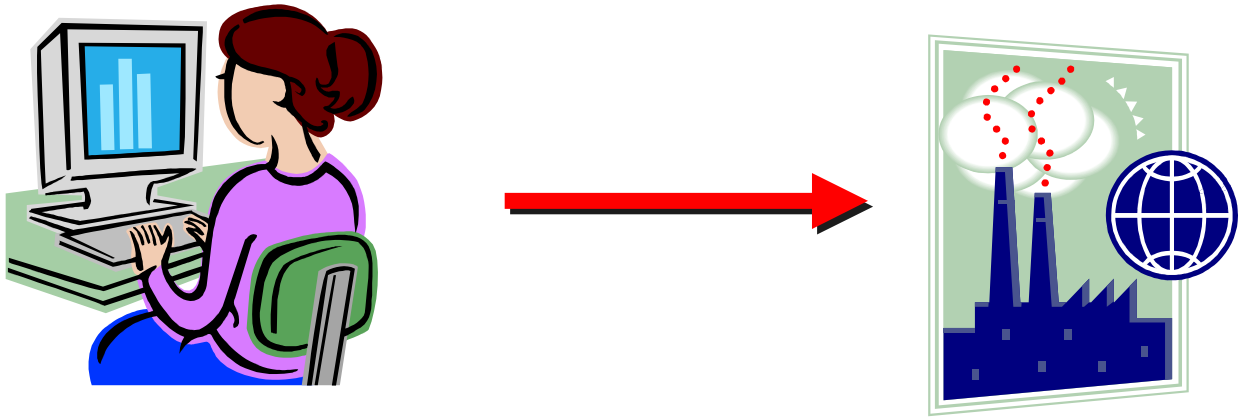

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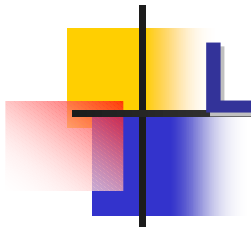

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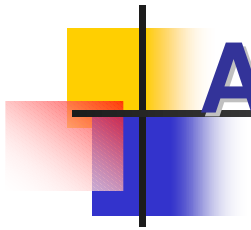

Architecture definition

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- instruction set specification (ISA)
- programming model
- operating system interface
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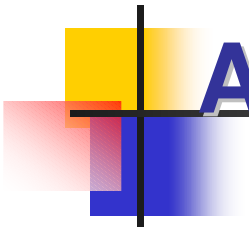

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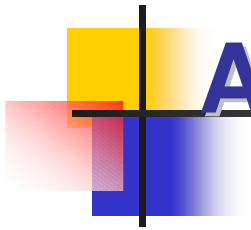

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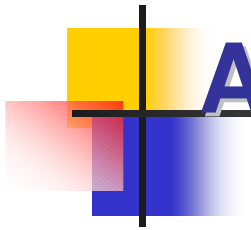

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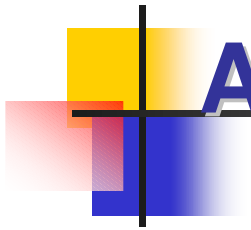

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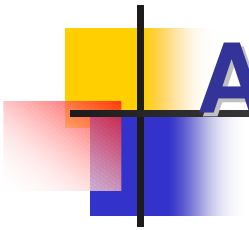

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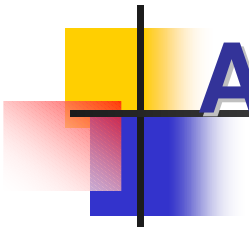

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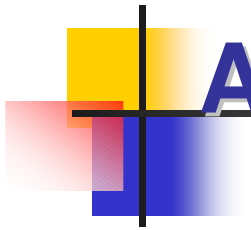

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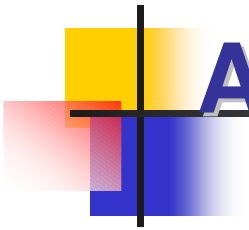

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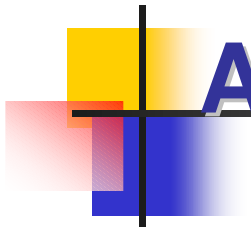

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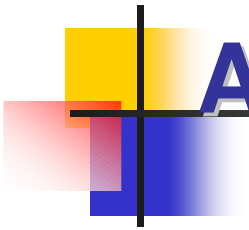

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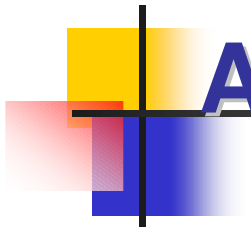

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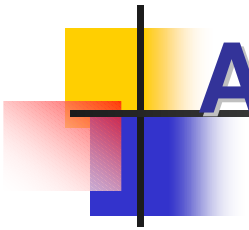

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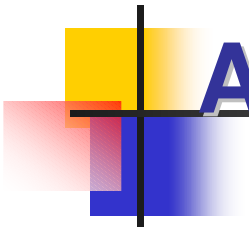

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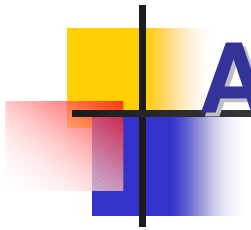

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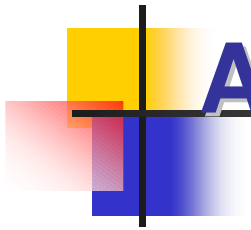

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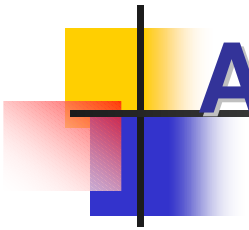

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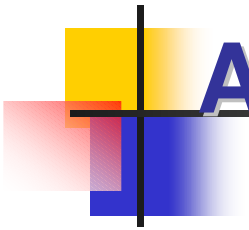

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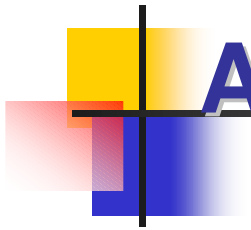

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- ARMv4
  - added half word load and store
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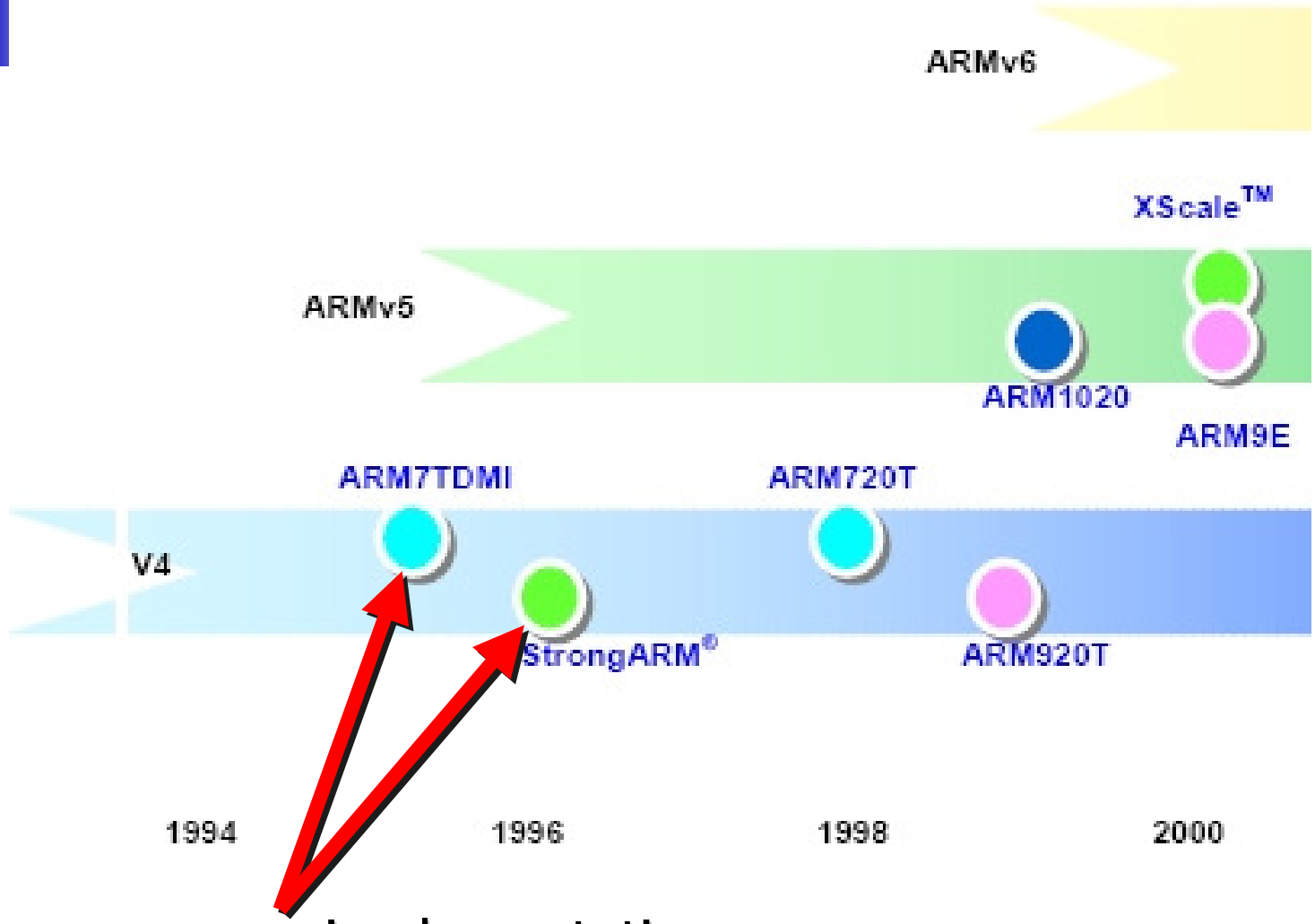

ARM architecture versions

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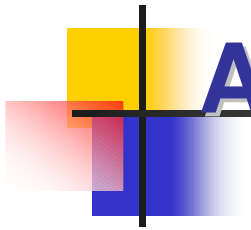

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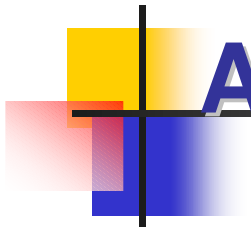

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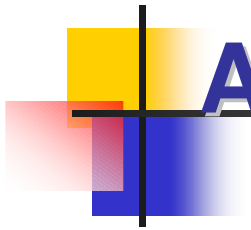

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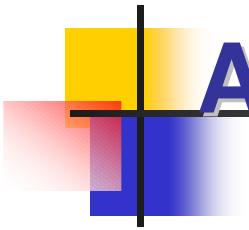

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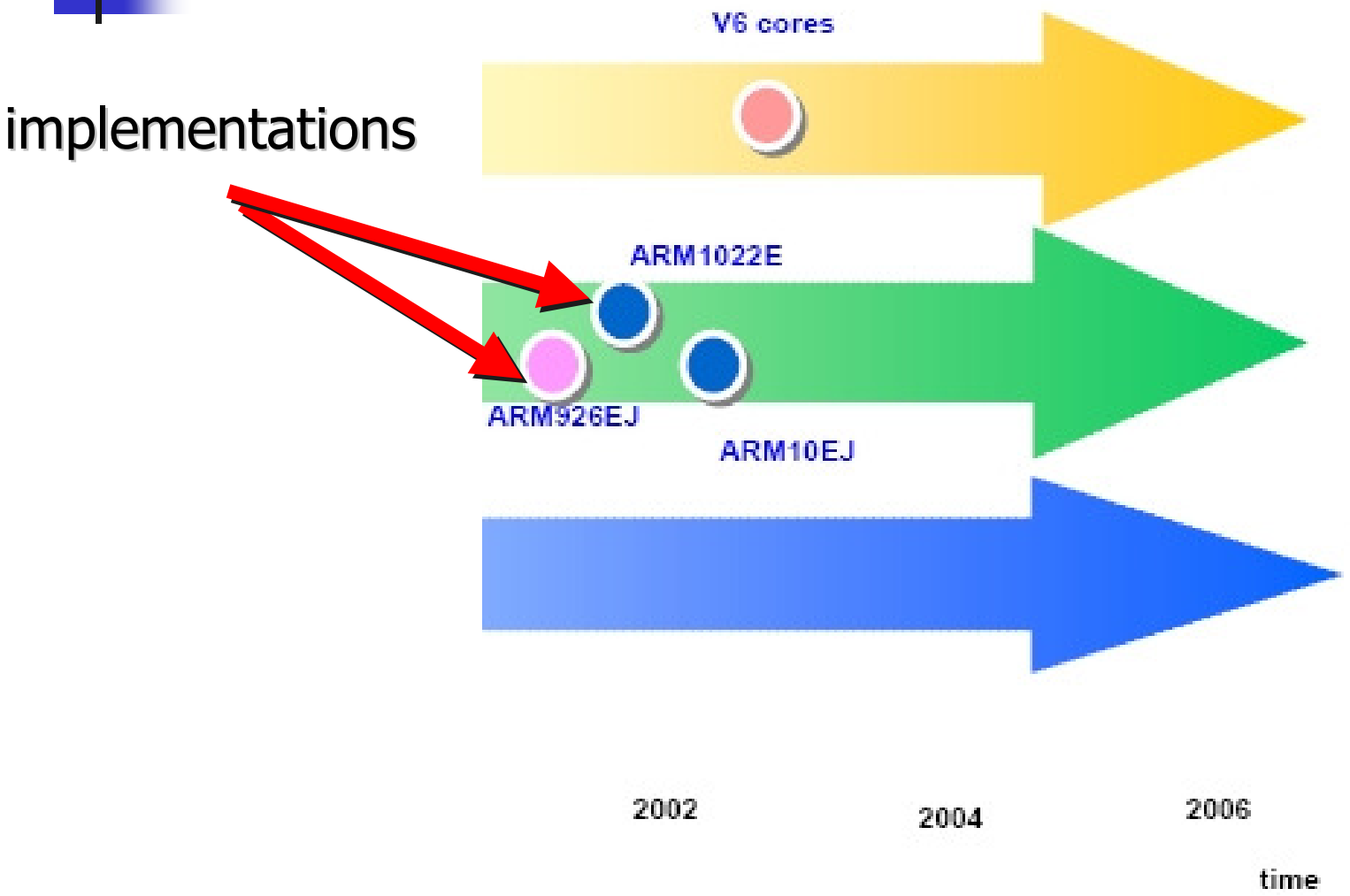

ARM ISA features

Based on Berkeley RISC design

- Features used:
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  - register windows
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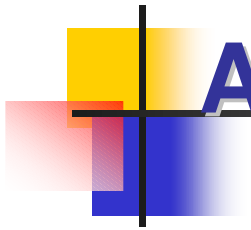

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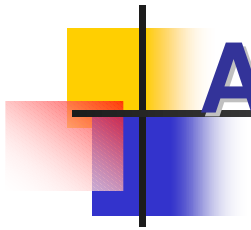

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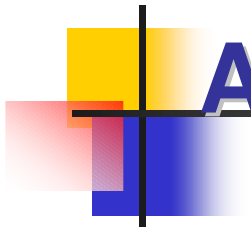

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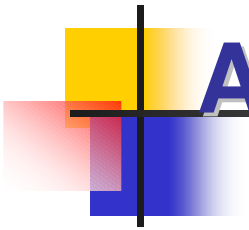

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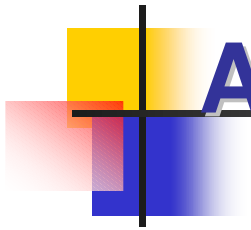

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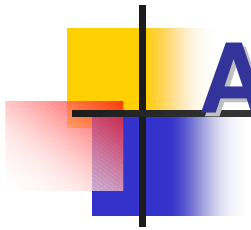

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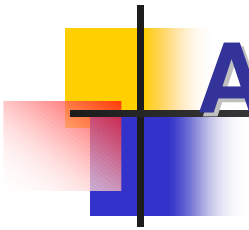

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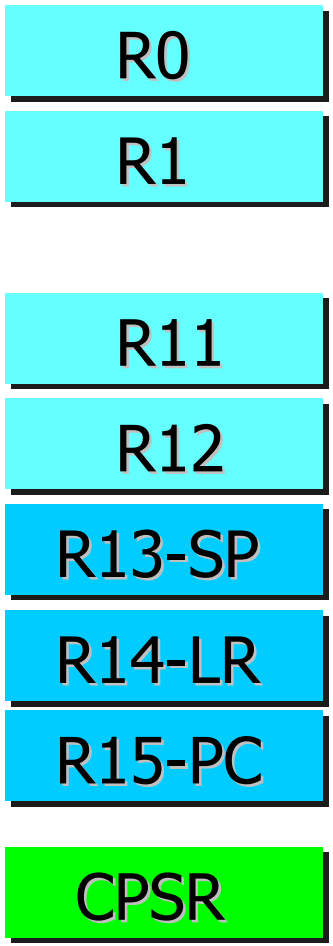

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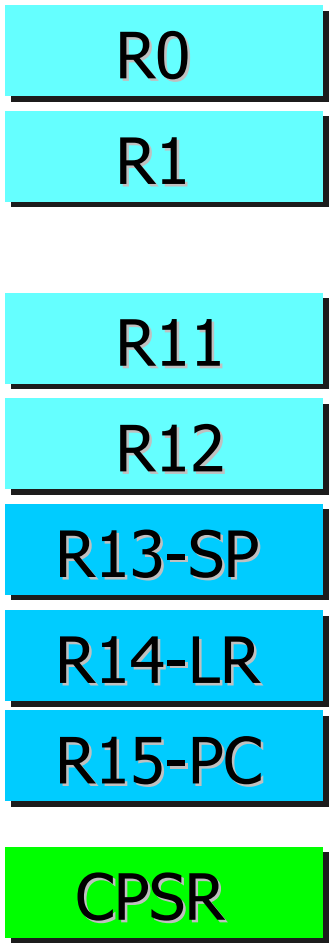

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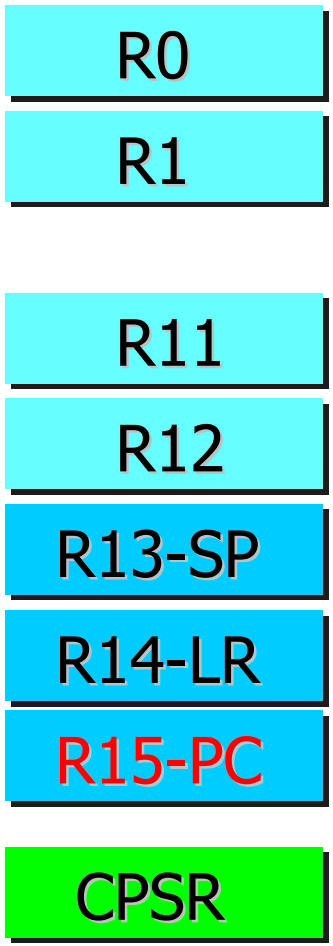

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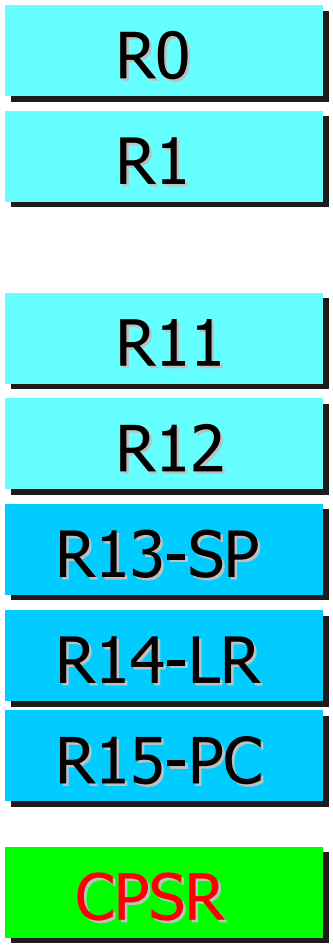

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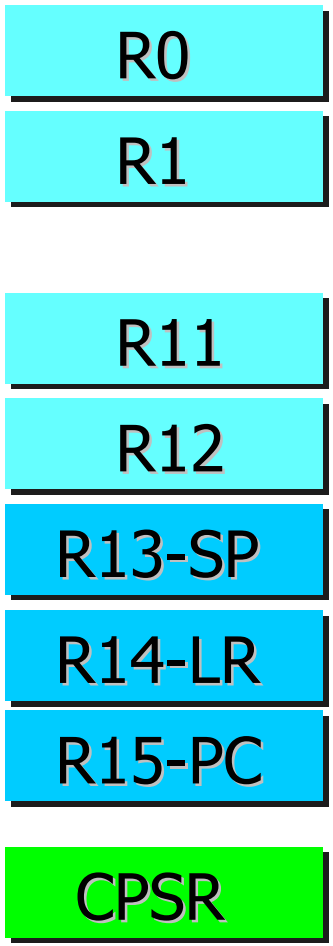

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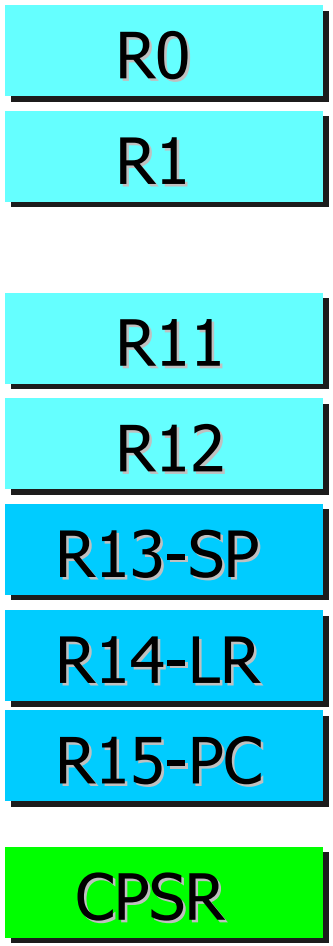

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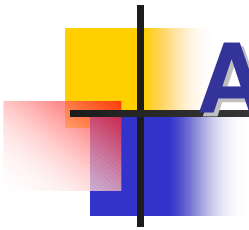
ARM coprocessor interface

- Supports a general-purpose extension of its instruction set through the addition of hardware coprocessors
- Support for up to 16 logical coprocessors
  - 16 private registers of any width
  - Coprocessors use load-store architecture
  - Coprocessors use handshaking to perform instructions



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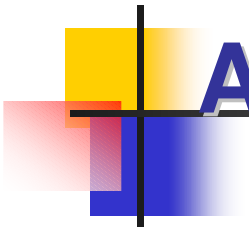

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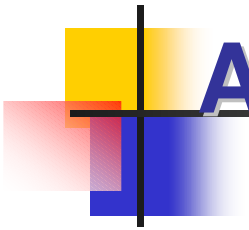

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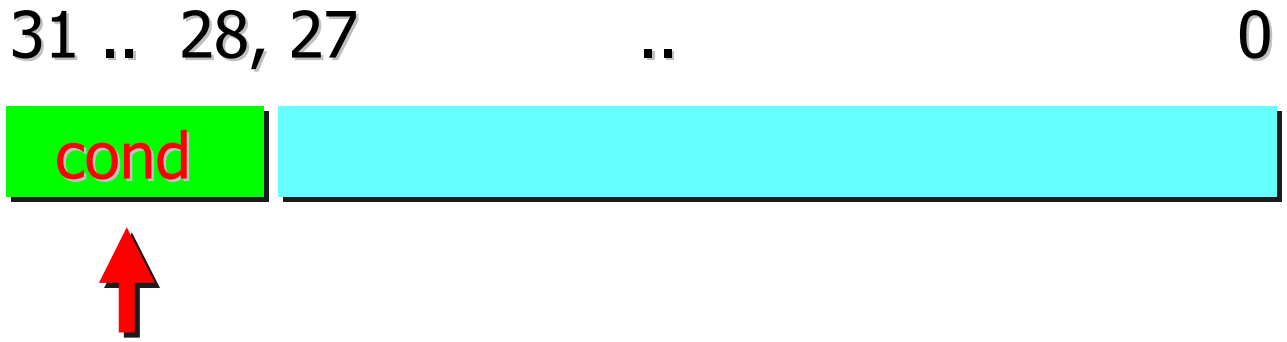

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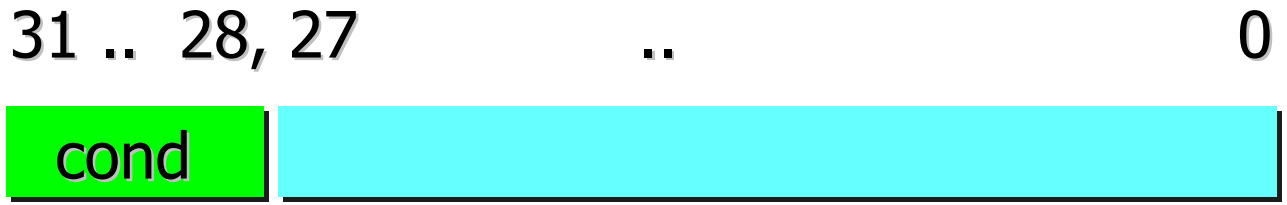

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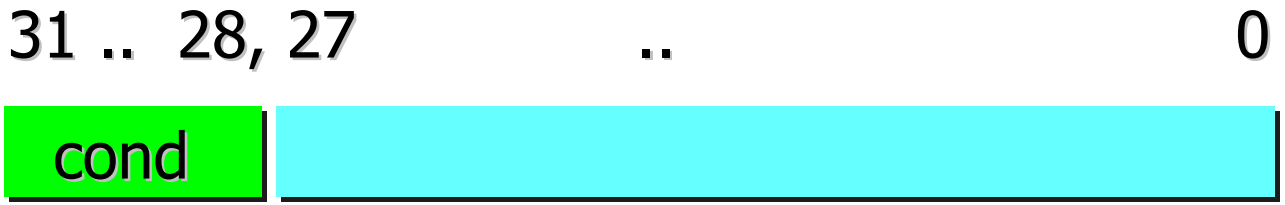

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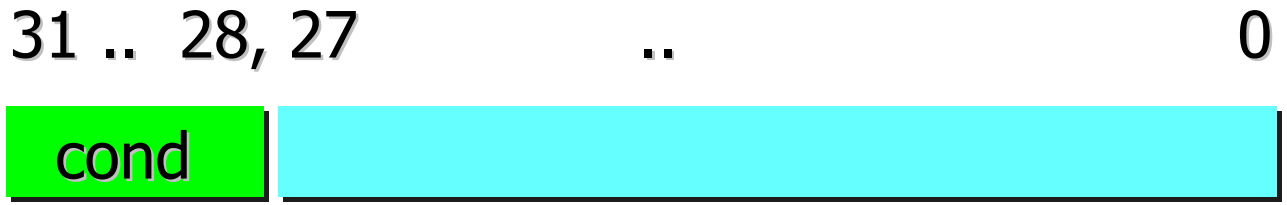

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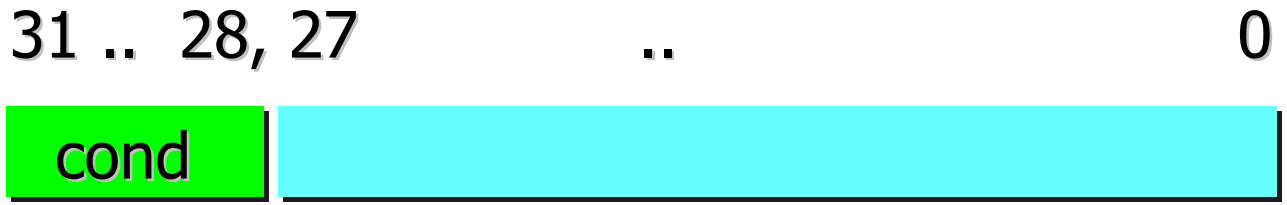

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subgt  Ri, Ri, Rj
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bne  loop
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3-address arithmetical instructions

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conditional branch instruction

Conditional execution

- conditional execution cuts down on the space available for displacement memory access
- avoids branch instructions for simple if statements

Conditional execution

```
int gcd(int i, int j)
{
while (i!=j)
{ if (i>j) i -=j;
else j -=i; }
return i;
}
```

b	test	
loop	subgt	Ri, Ri, Rj
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- Any subset (or all) of the 16 registers visible in the current operating mode to be loaded from or stored to memory
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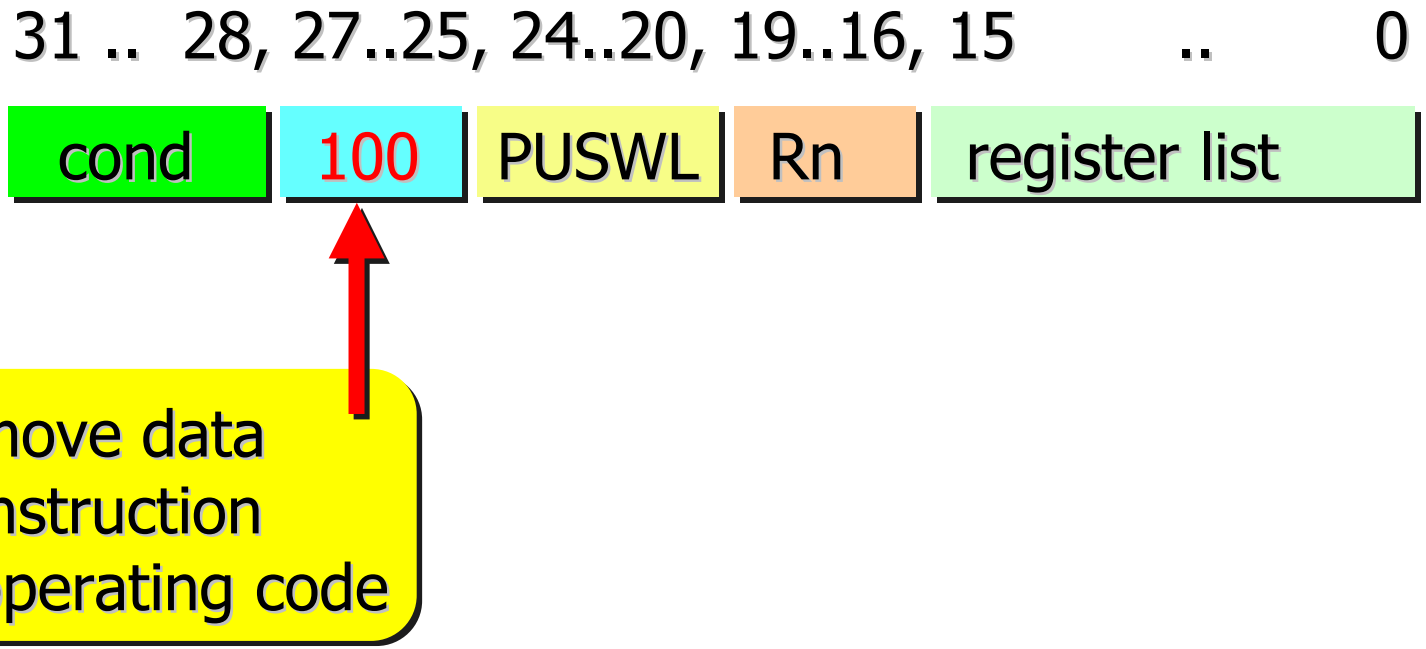

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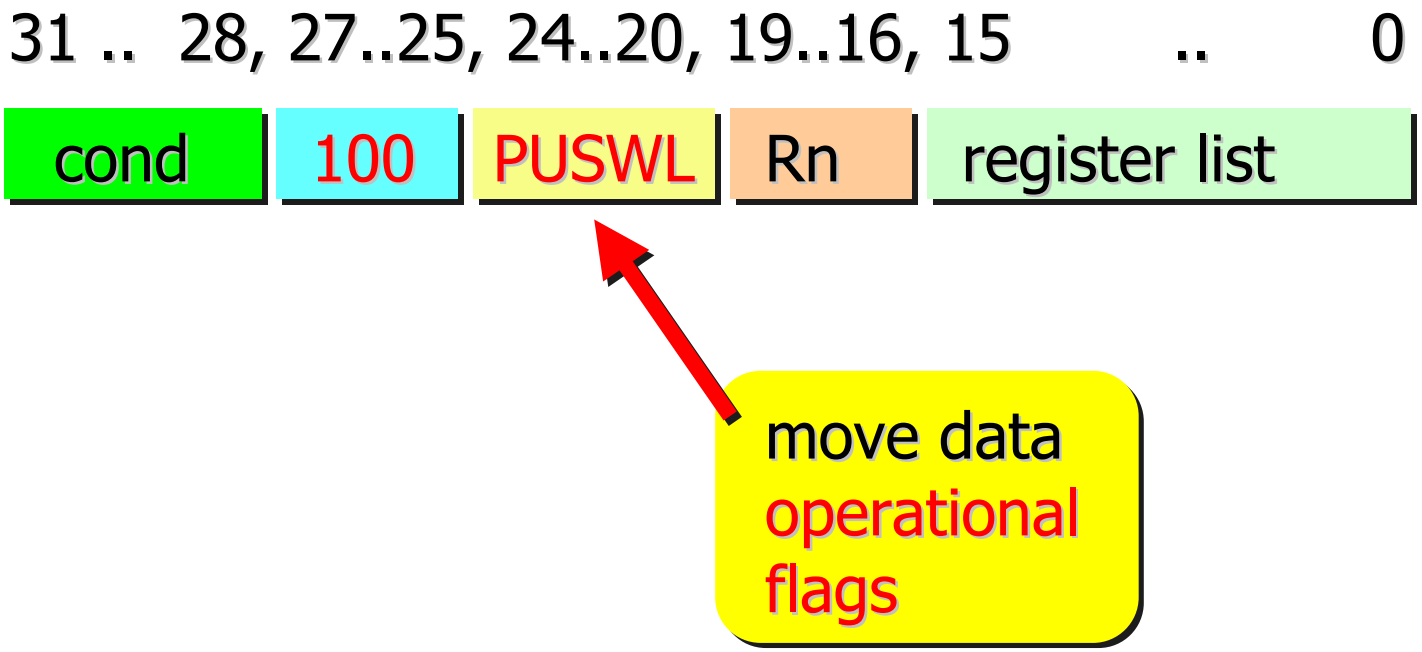

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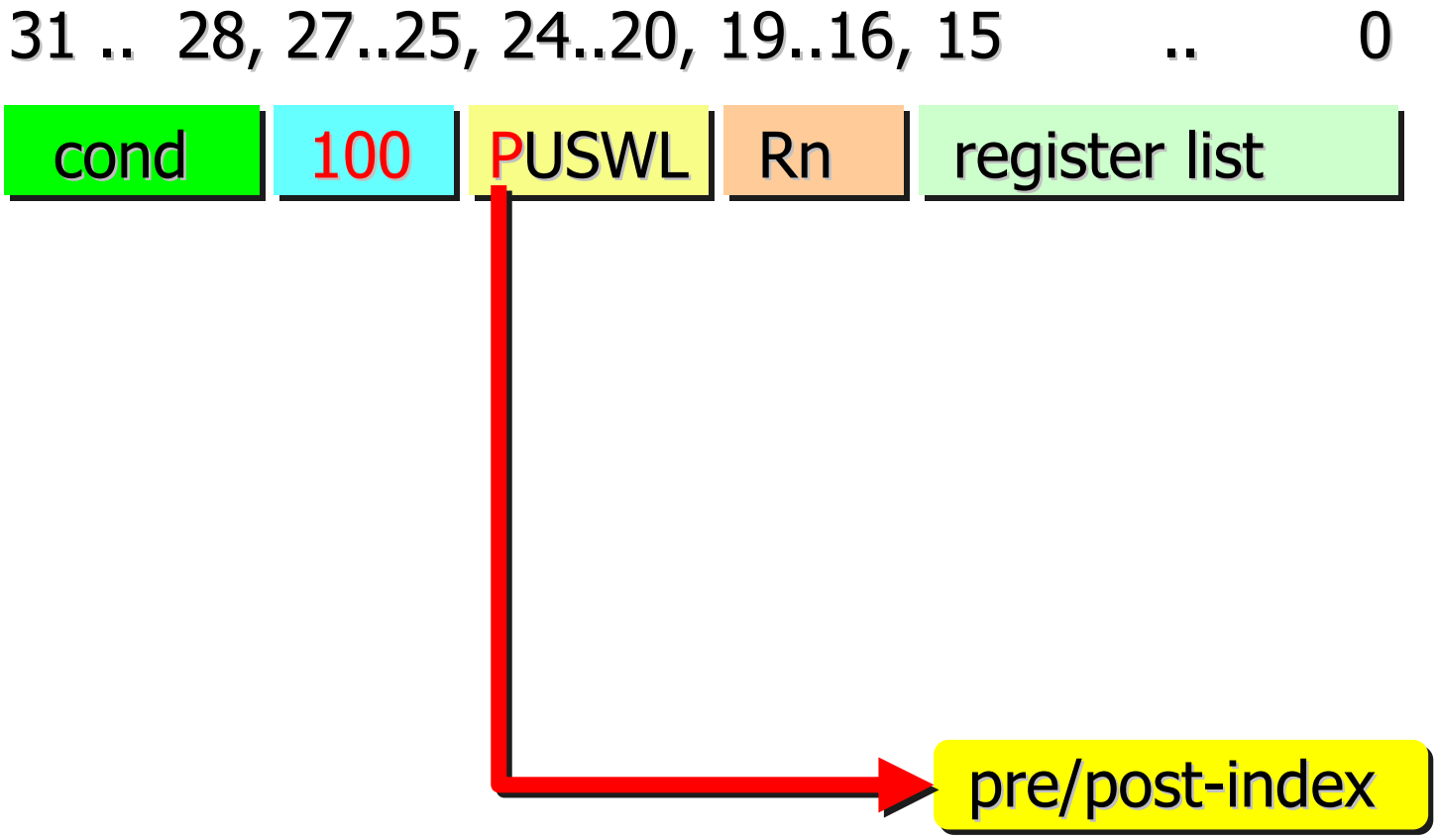

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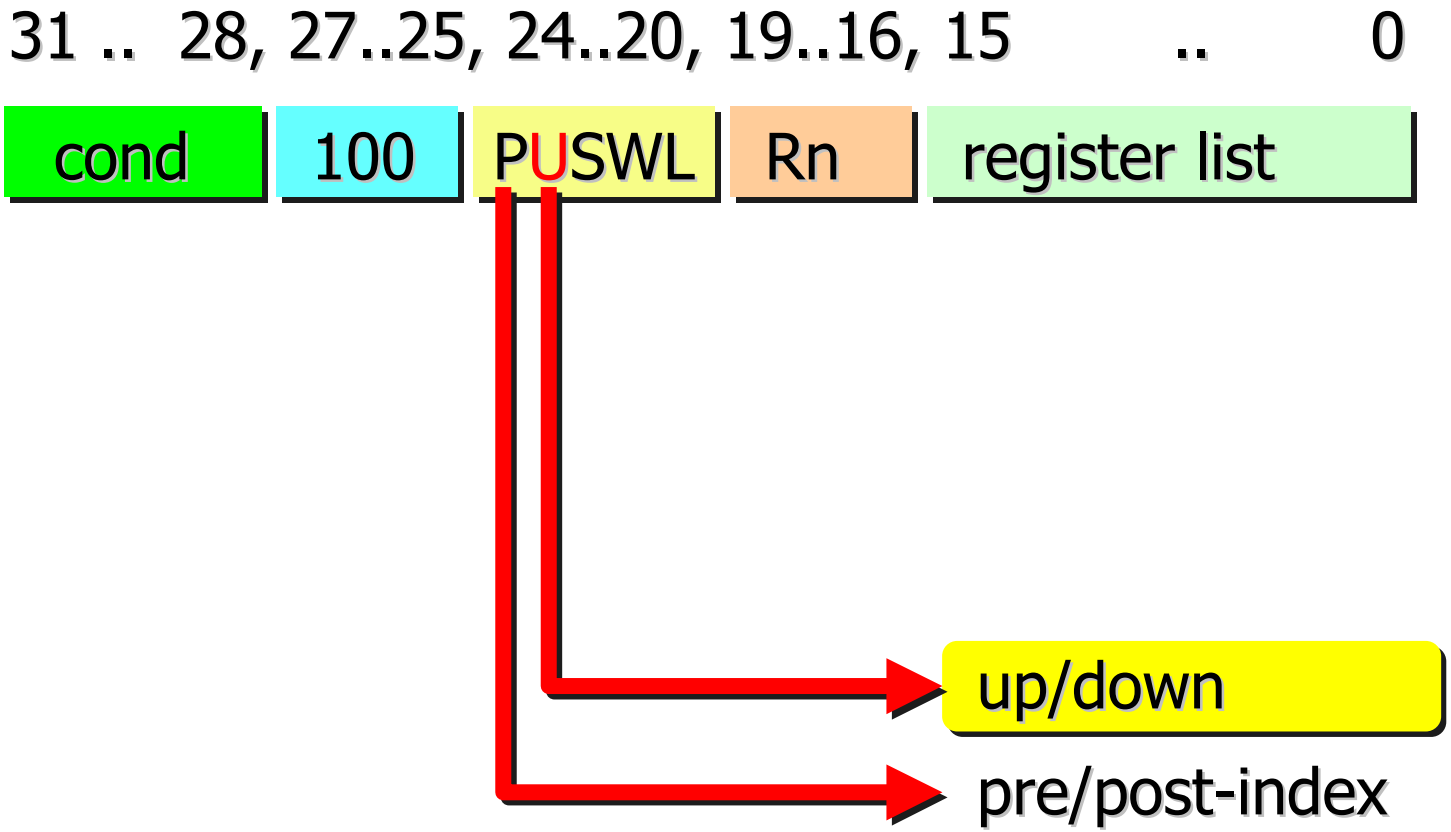

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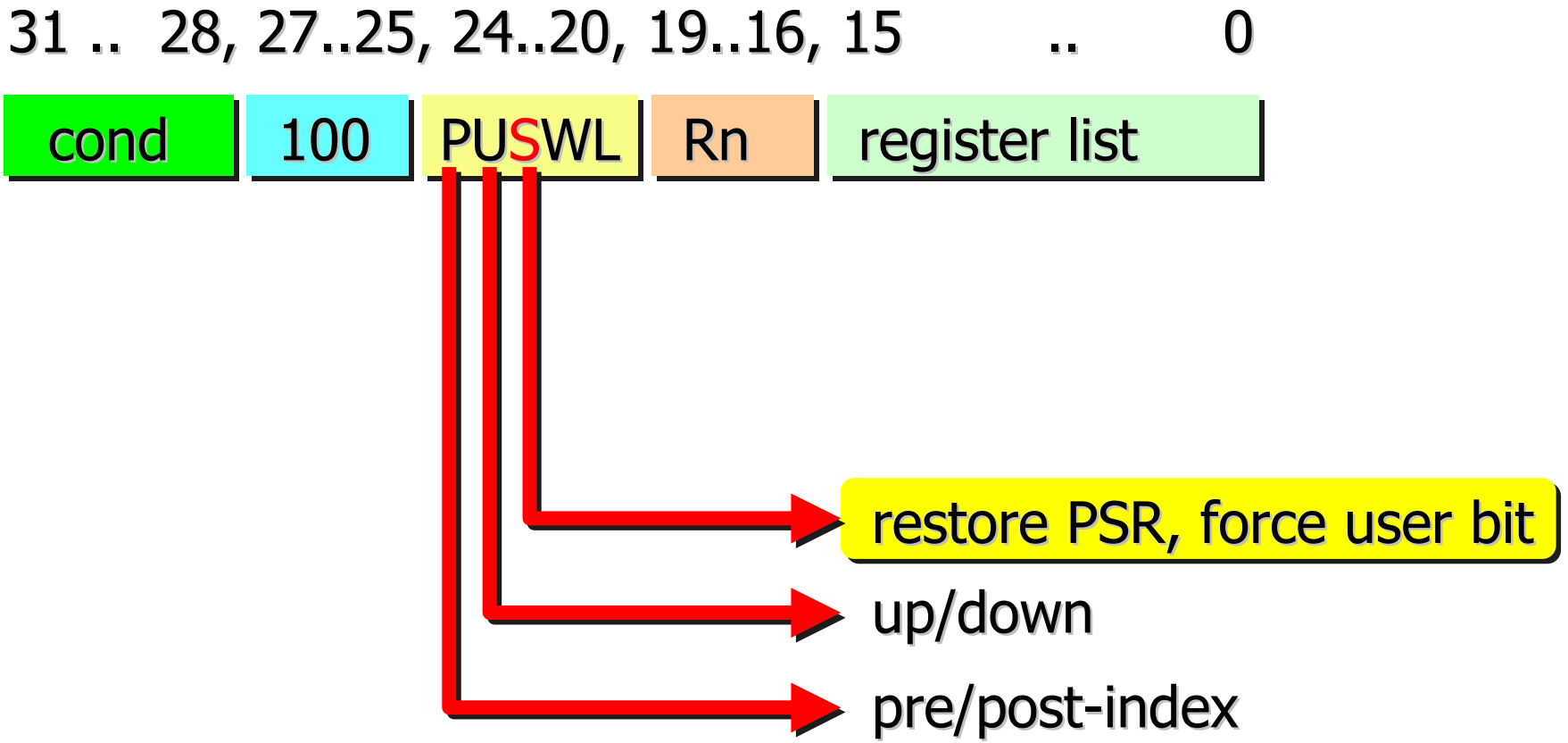

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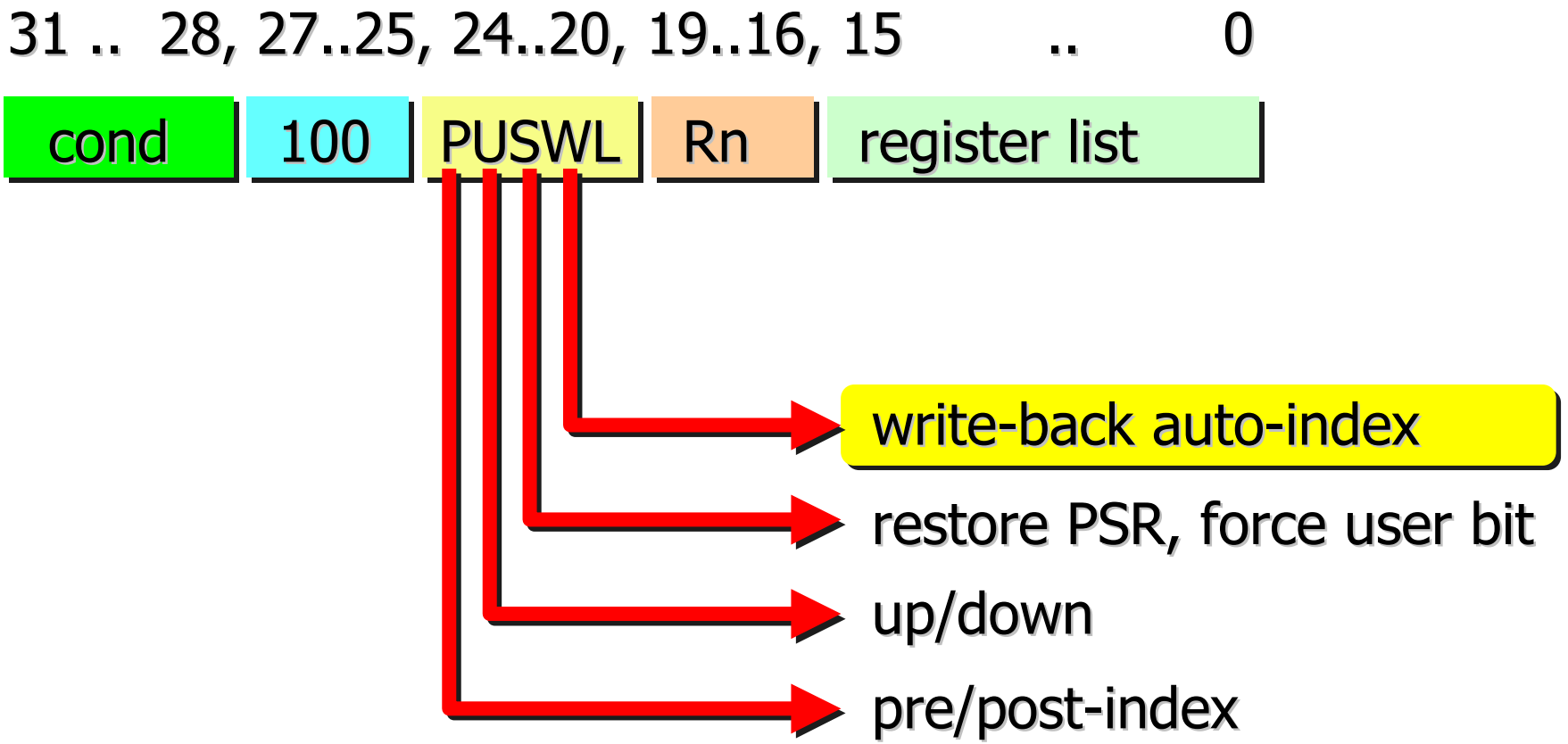

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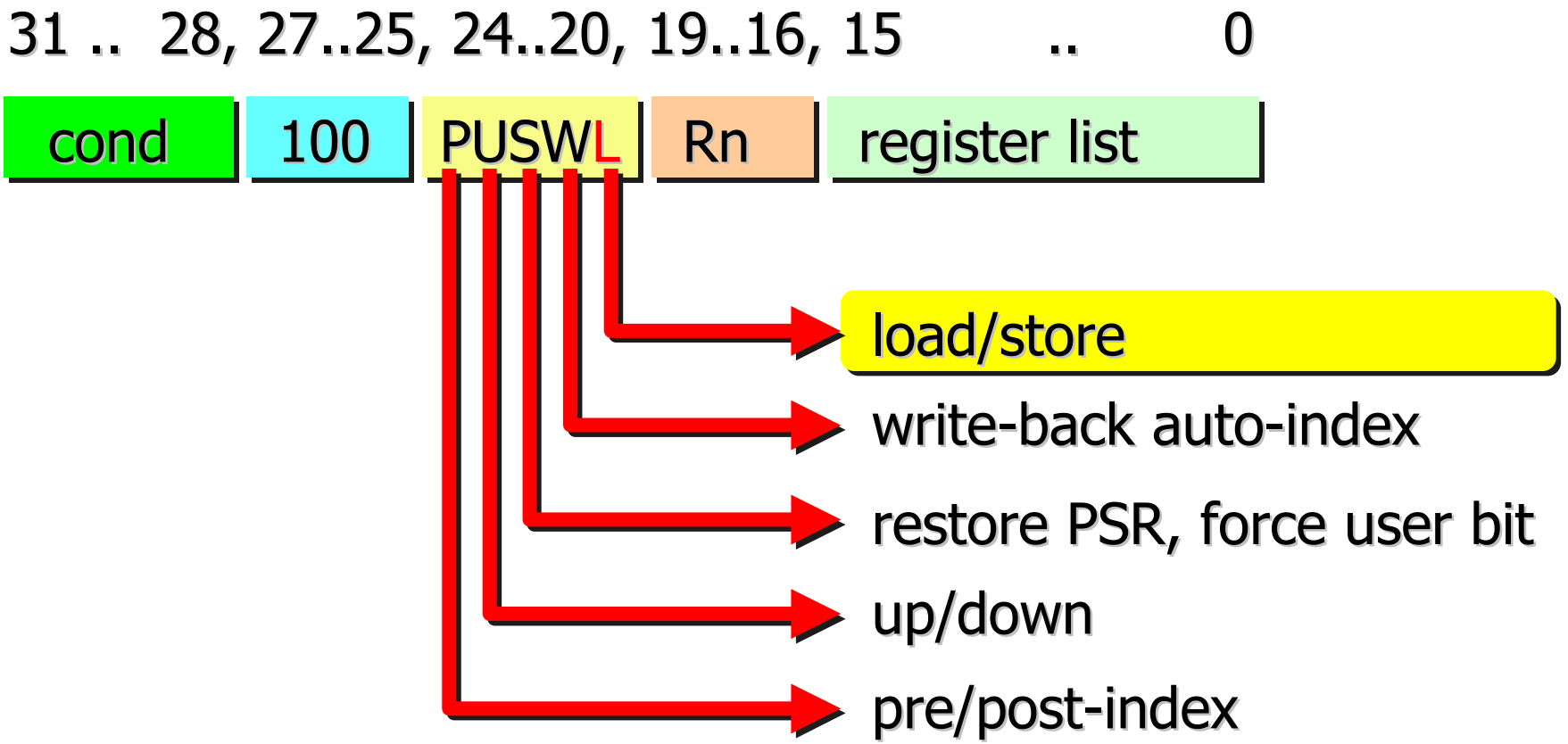

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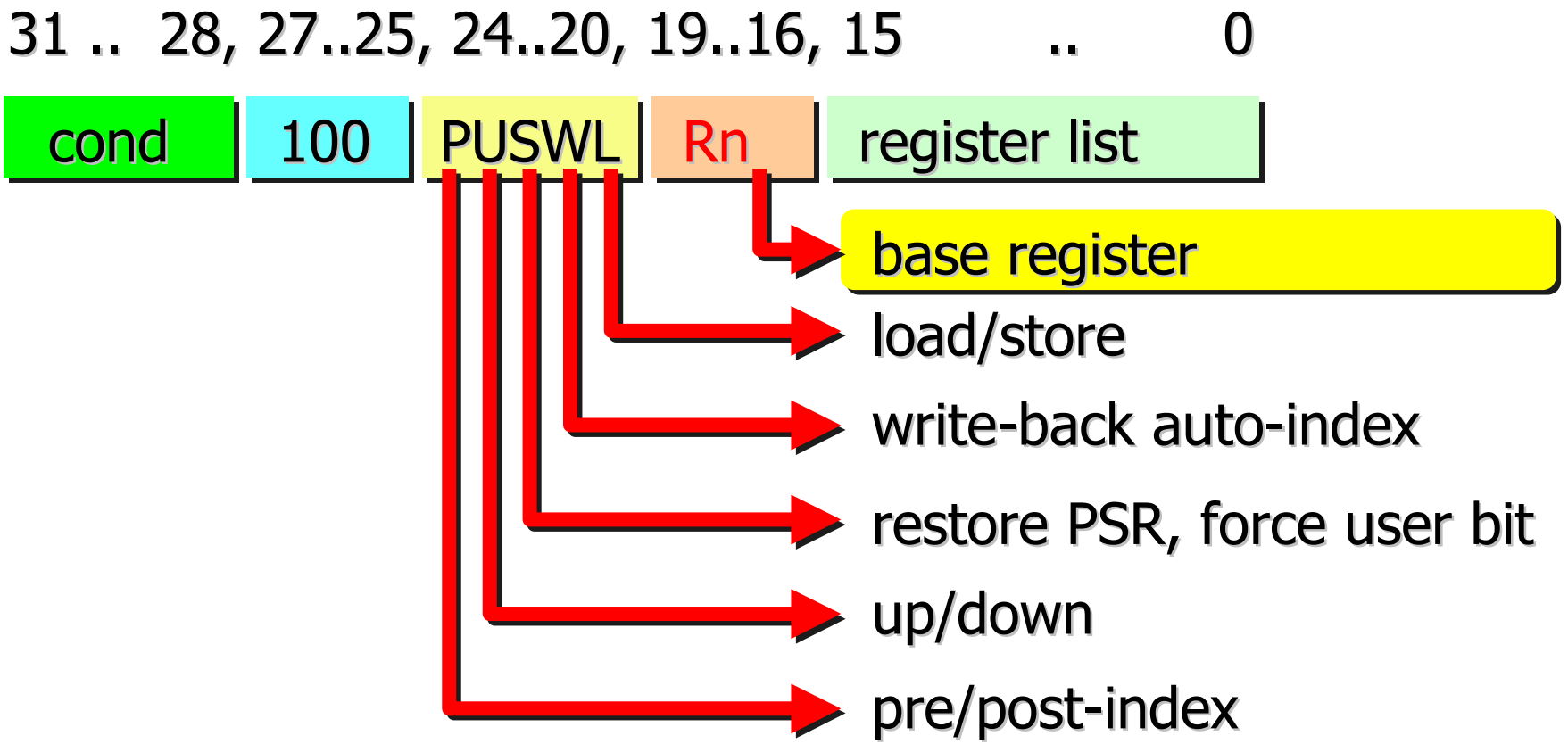

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Architectural support for OS

- coprocessor number 15
- on-chip system OS control processor controls:
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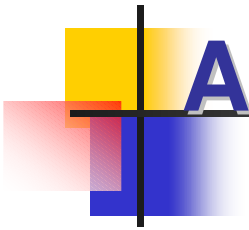

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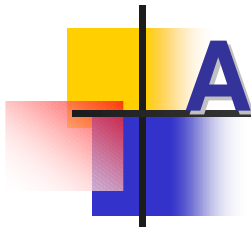

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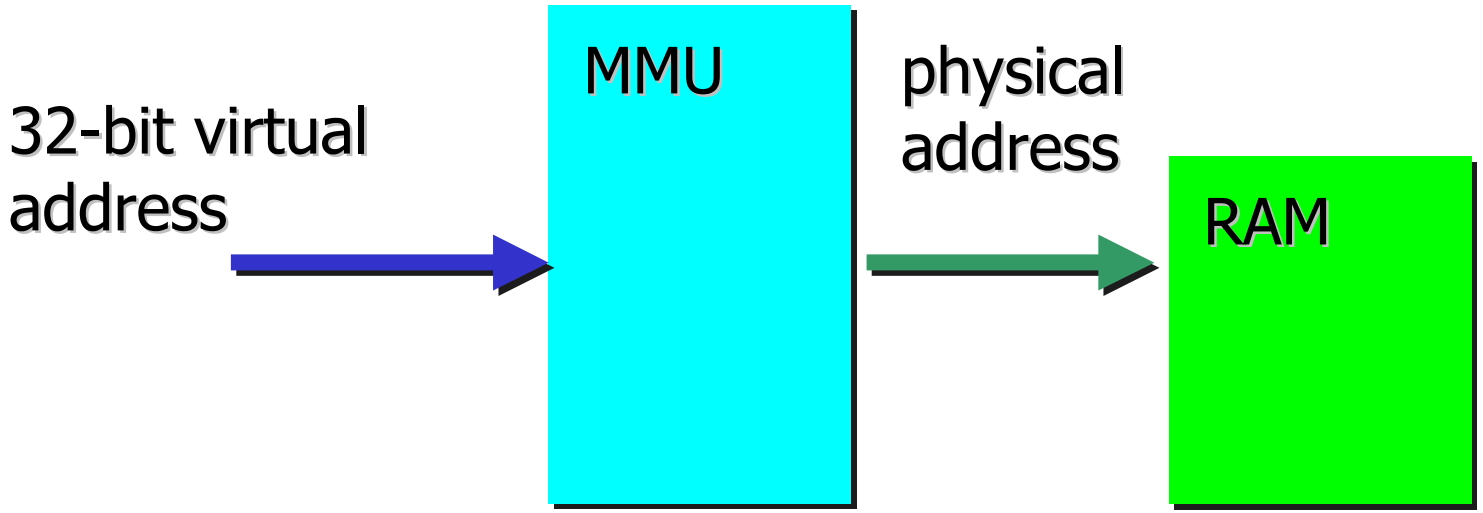
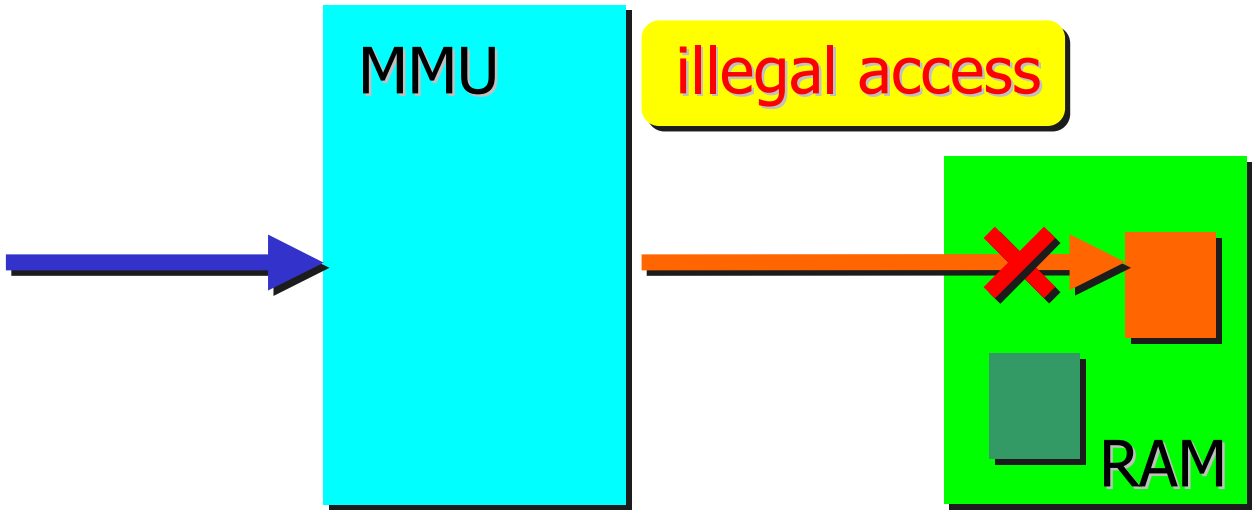


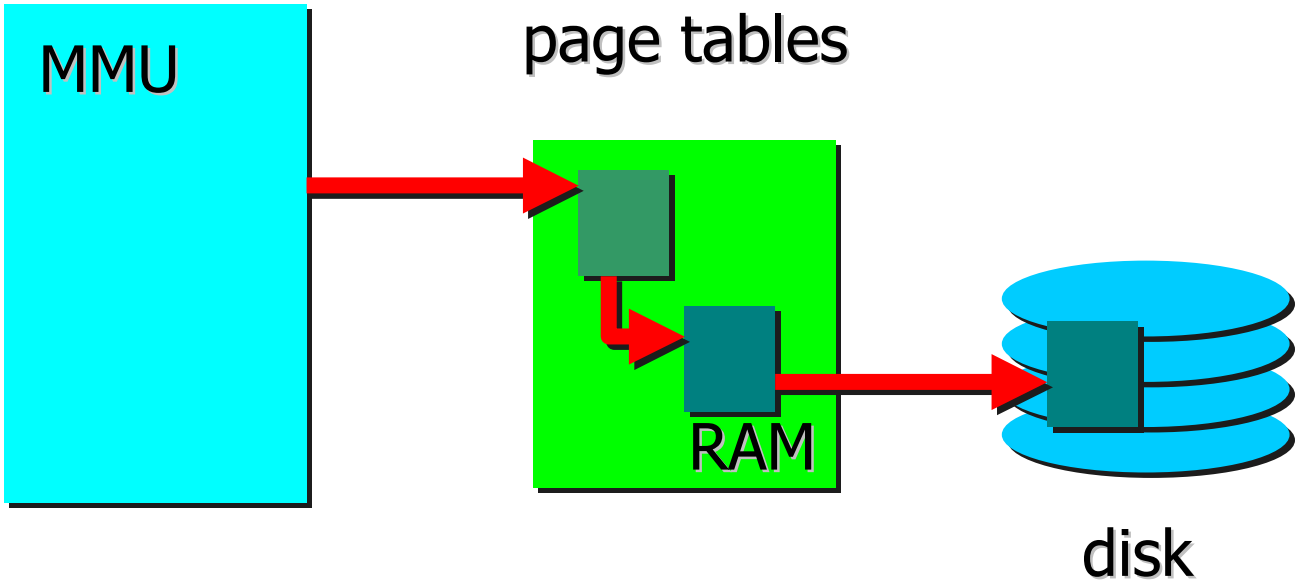
MMU architecture operations

- translates virtual addresses into physical addresses
- controls memory access permissions, aborting illegal accesses



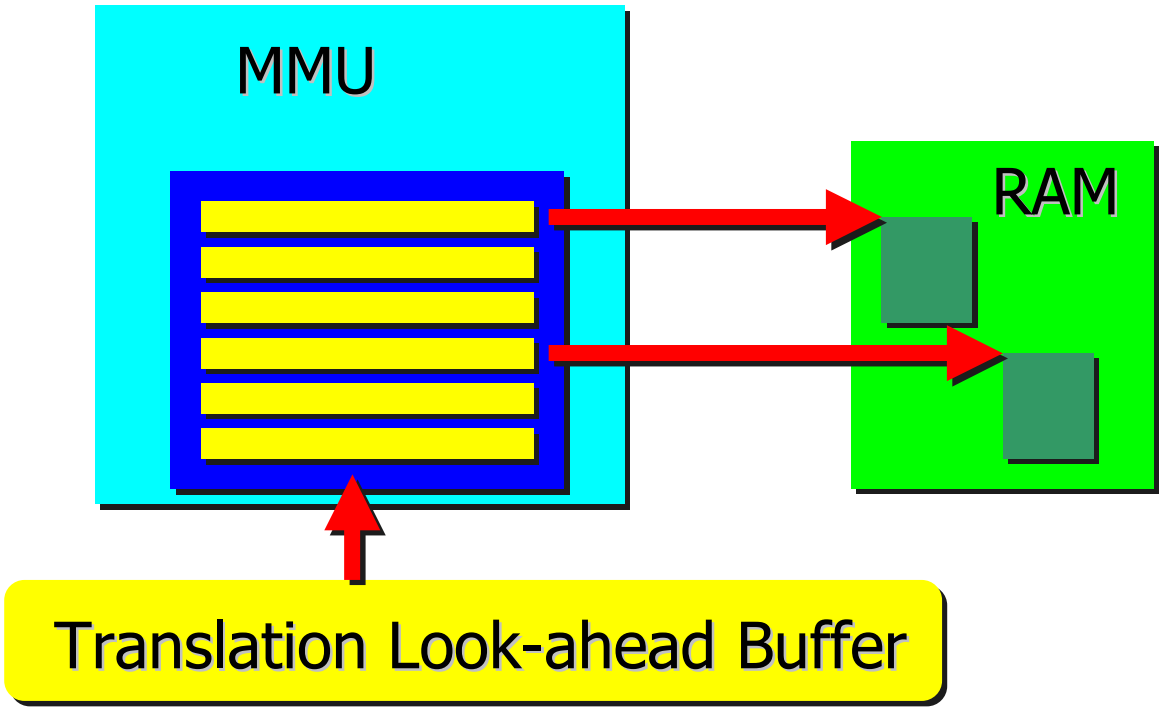
MMU architecture operations

- uses two-level page table with table-walking hardware



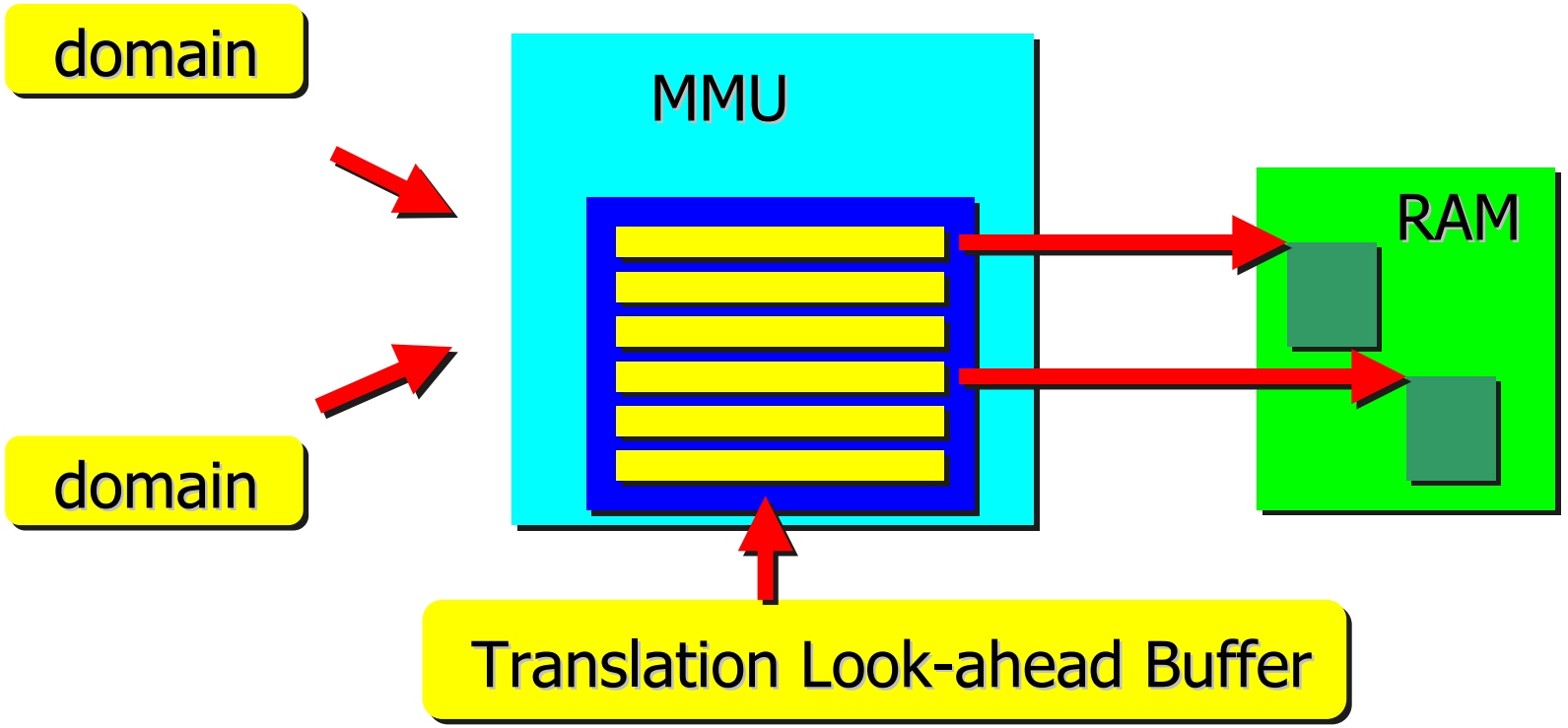
MMU architecture operations

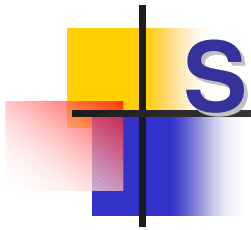
- controls a TLB which stories recently used page translations



MMU architecture operations

- provides 16 domains – each protected from one another while using the same TLB





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Synchronization problem:

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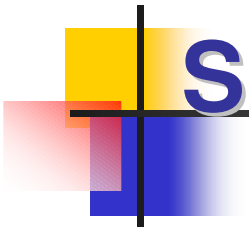

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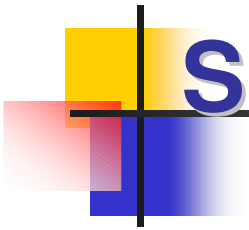

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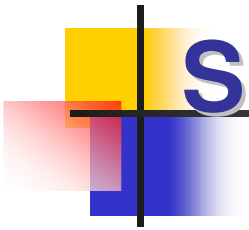

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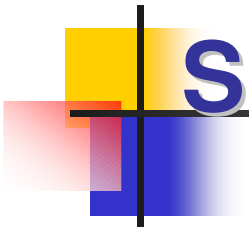

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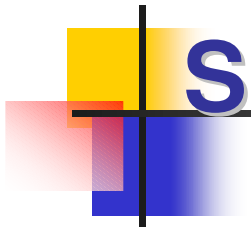

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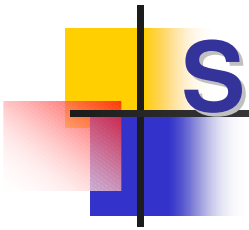

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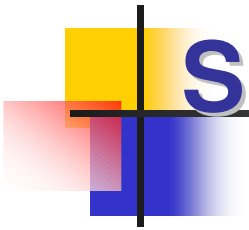

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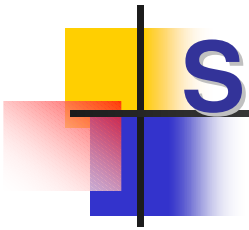

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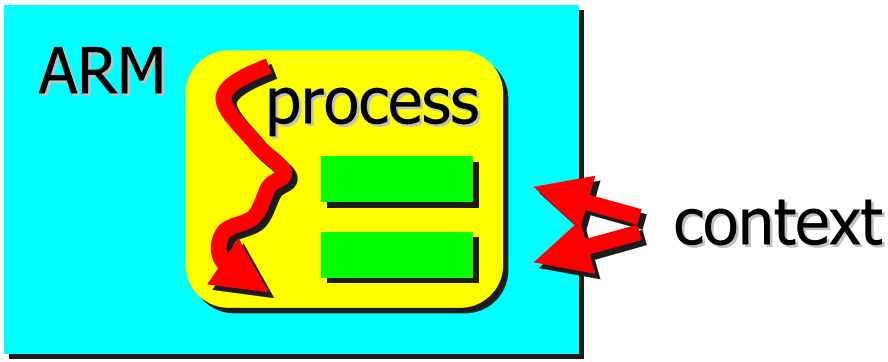

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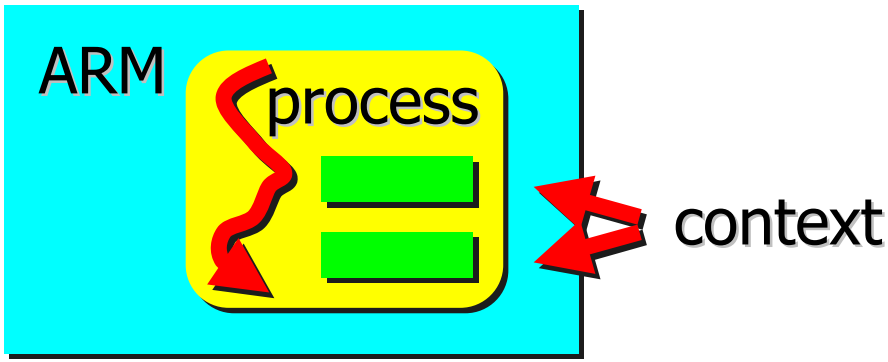

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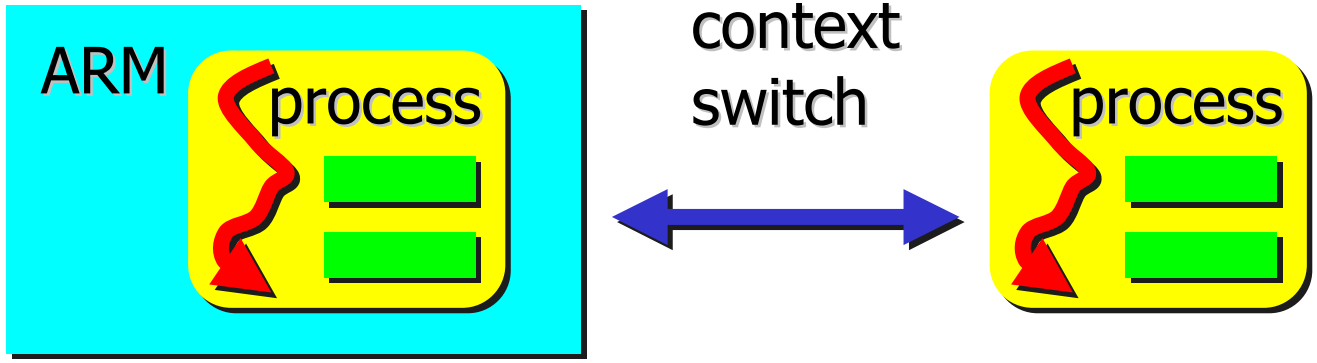

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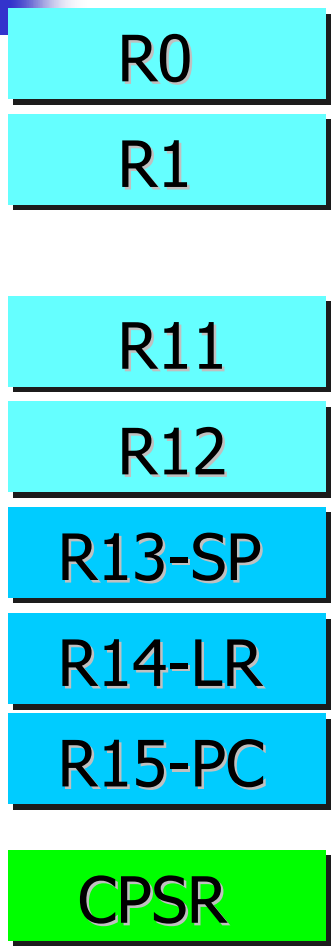

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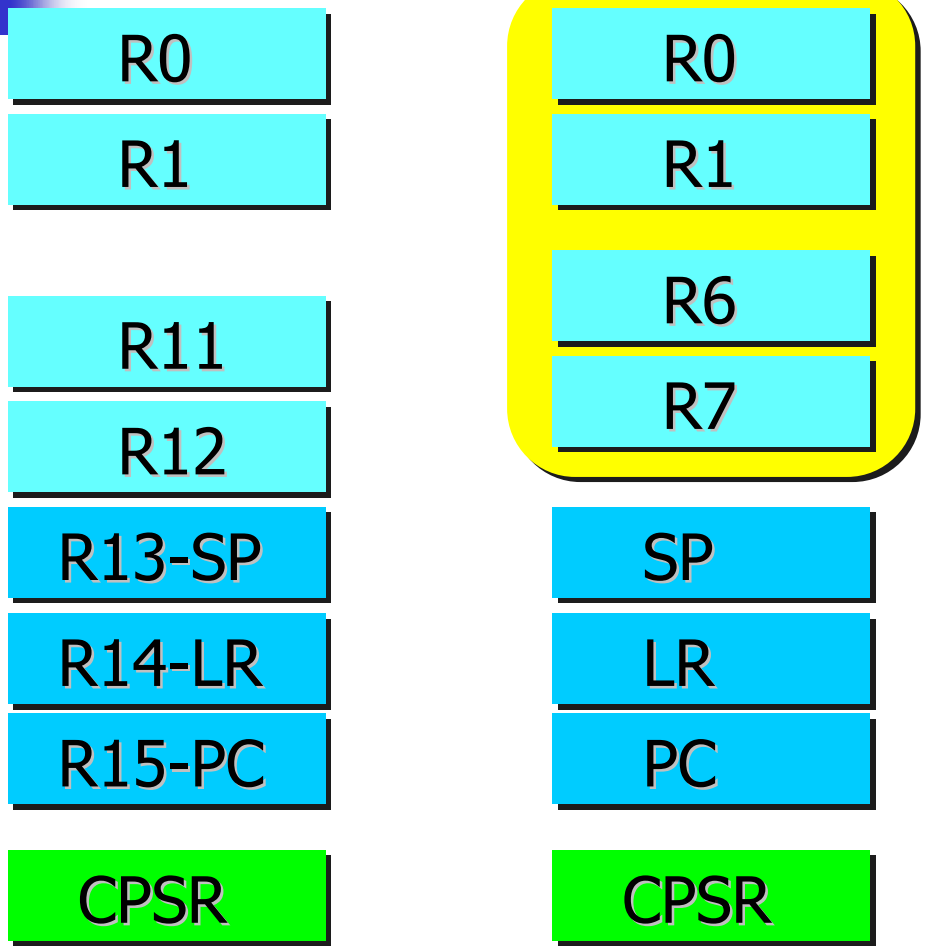

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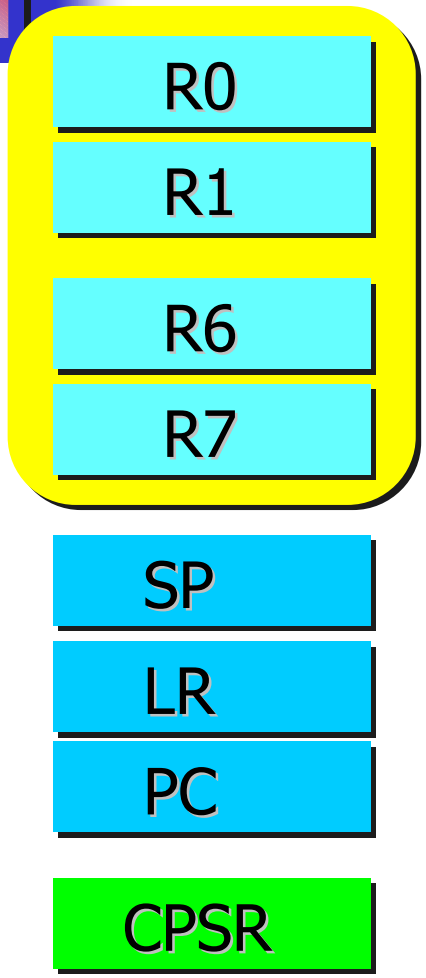

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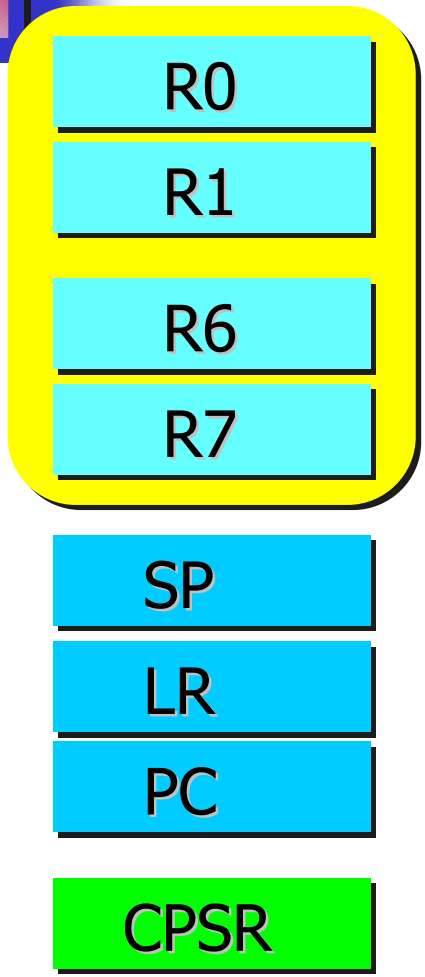

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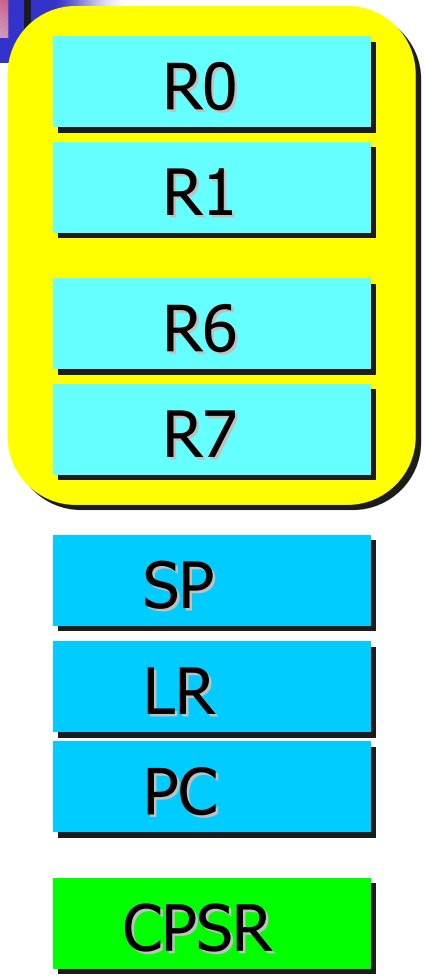

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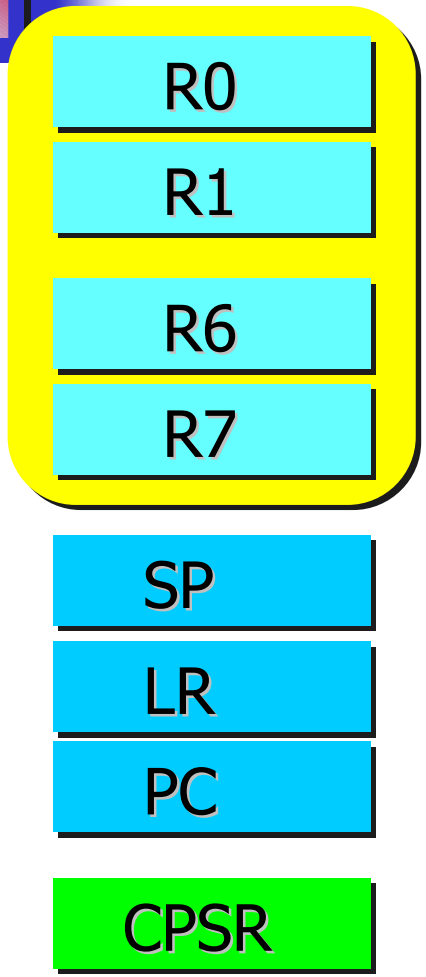

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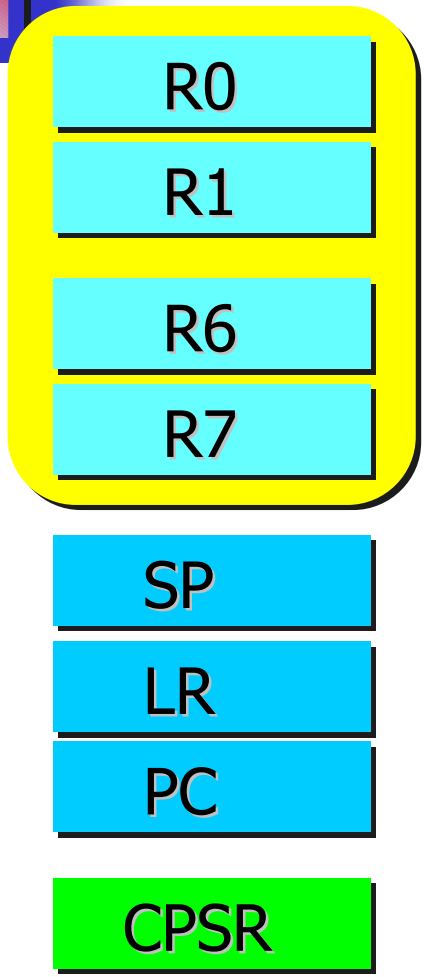

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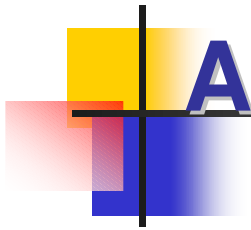

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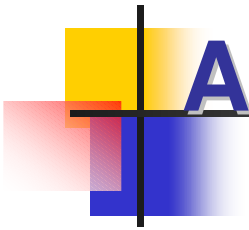

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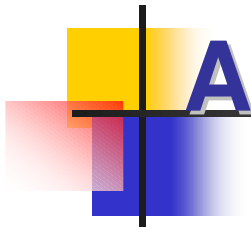

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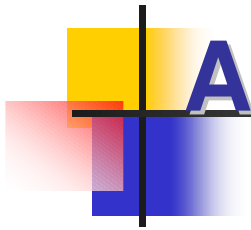

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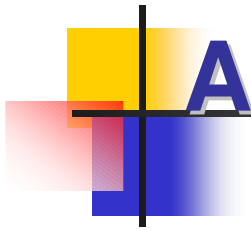

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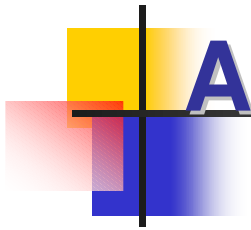

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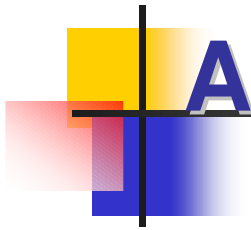

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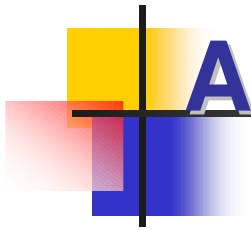

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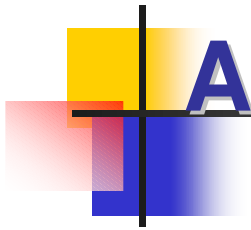

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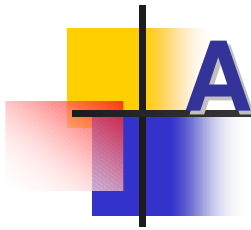

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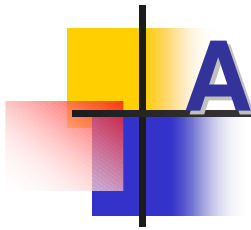

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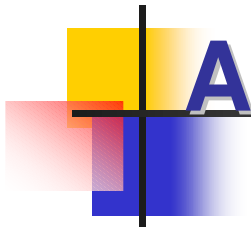

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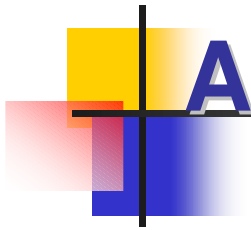

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  - to execute directly Java Byte Code
  - reuse of all existing processor resources without the need to re-engineer existing architecture
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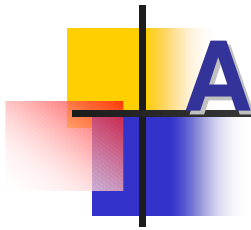

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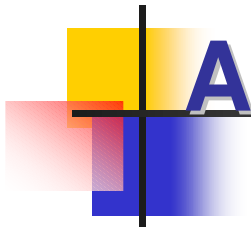

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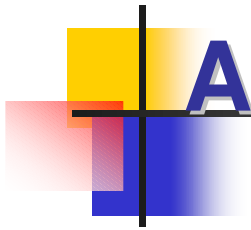

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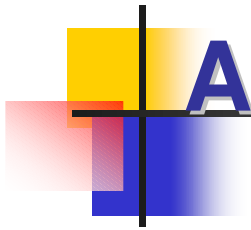

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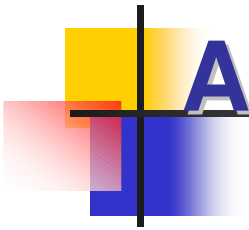

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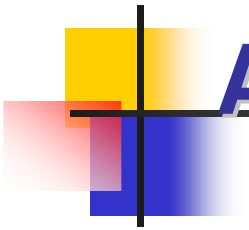

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- unaligned and mixed-endian data support
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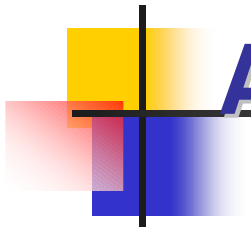

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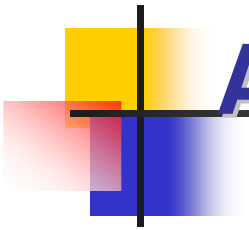

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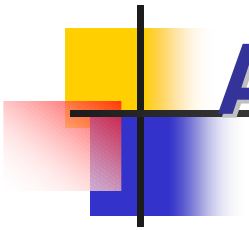

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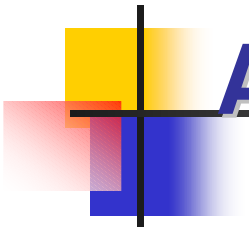

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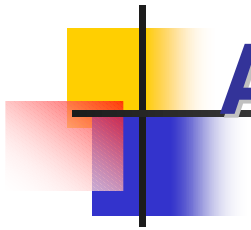

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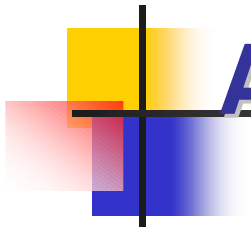

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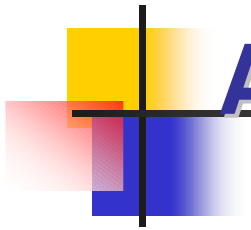

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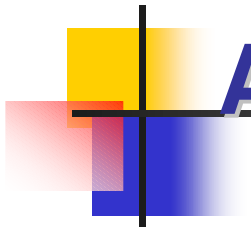

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- over 60 SIMD instructions
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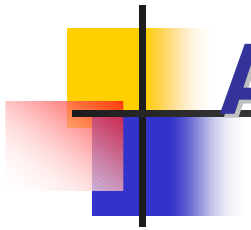

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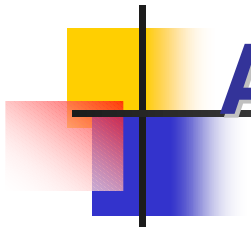

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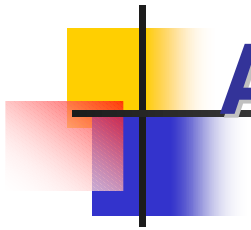

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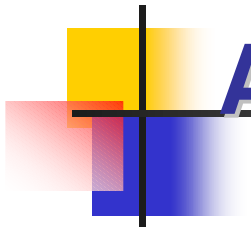

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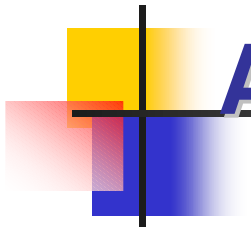

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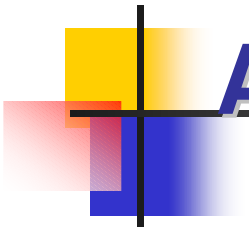

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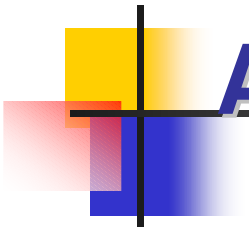

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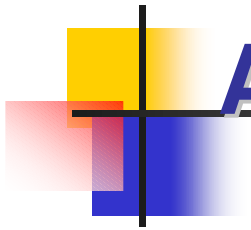

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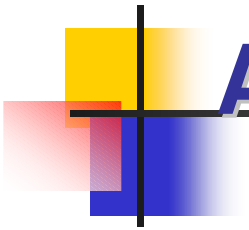

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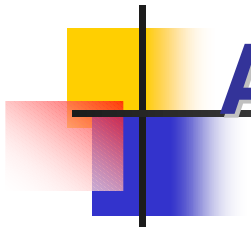

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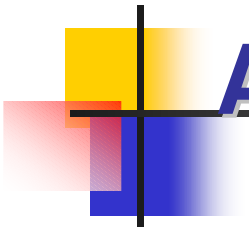

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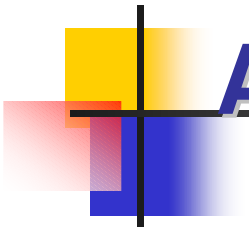

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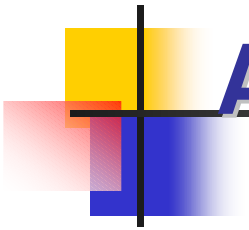

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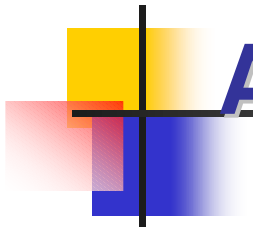
V3	ARM7, ARM700, ARM710
V4T	ARM7TDMI, ARM710T, ARM720T, ARM740T
V4	StrongARM, ARM8, ARM810
V5	ARM9TDMI, ARM920T, ARM940T
V5TE	ARM9E-S, ARM10TDMI, ARM1020E, XScale
V6	ARM11



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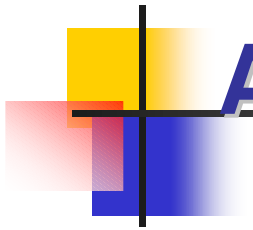

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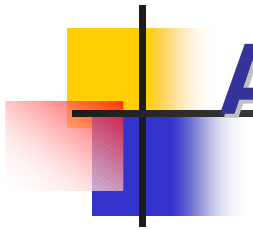

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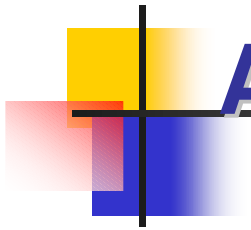

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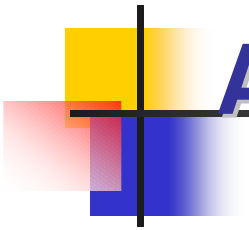

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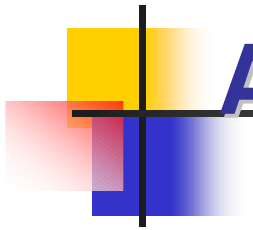

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- fetch: instruction is fetched from memory and placed in instruction pipeline
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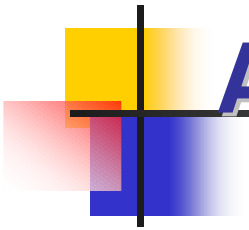

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- register bank: two read ports and one write port
- one additional read and one additional write port for R15
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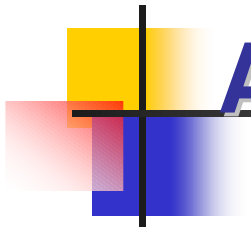

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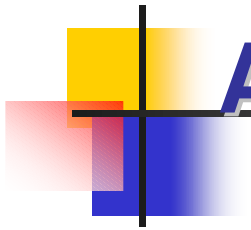

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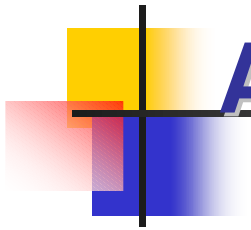

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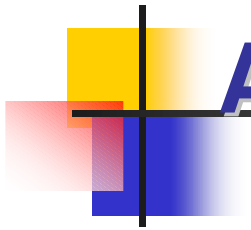

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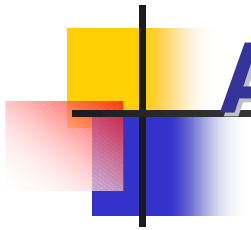

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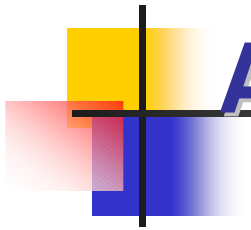

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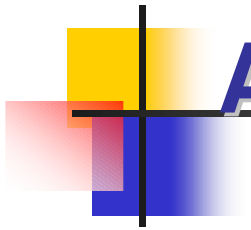

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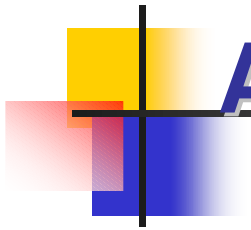

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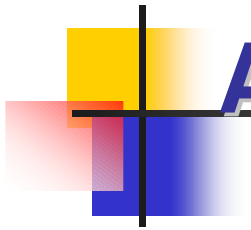

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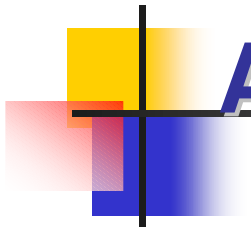

ARM9TDMI - StrongARM

- StrongARM has a dedicated branch adder which operates in parallel with the register read stage
- ARM9TDMI uses the main ALU – an additional clock cycle penalty for a taken branch but smaller core
- StrongARM designed for particular technology
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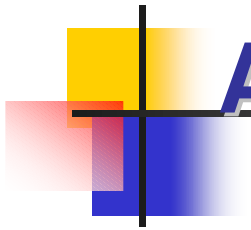

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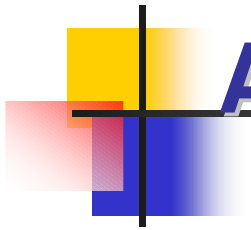

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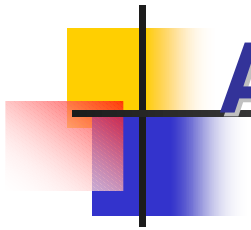

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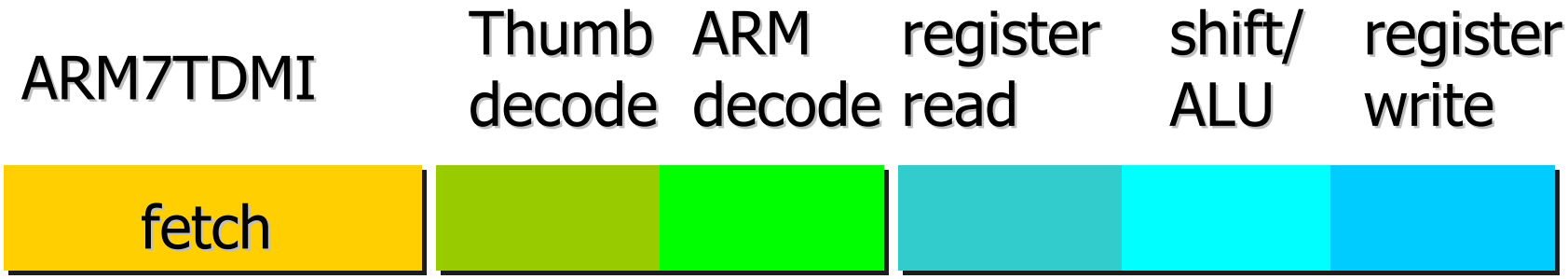

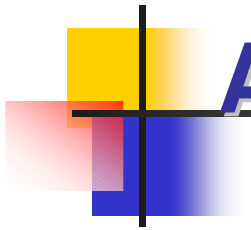

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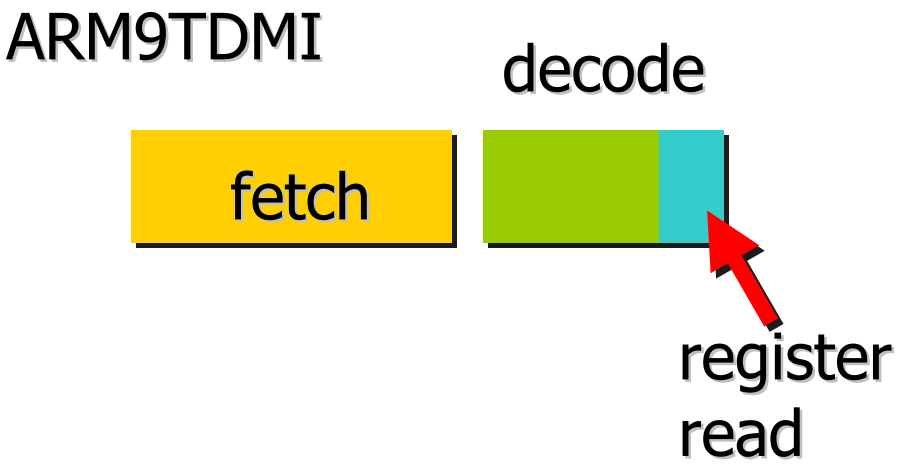

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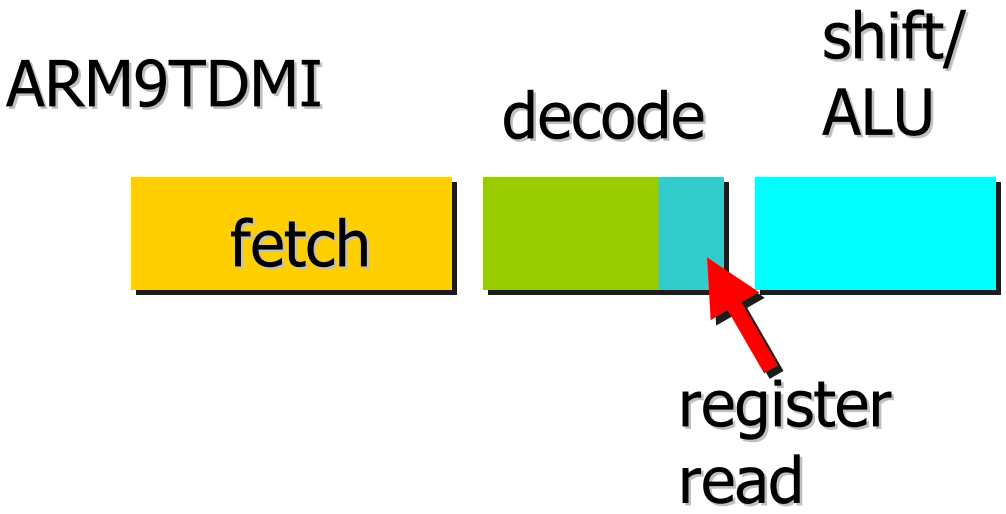

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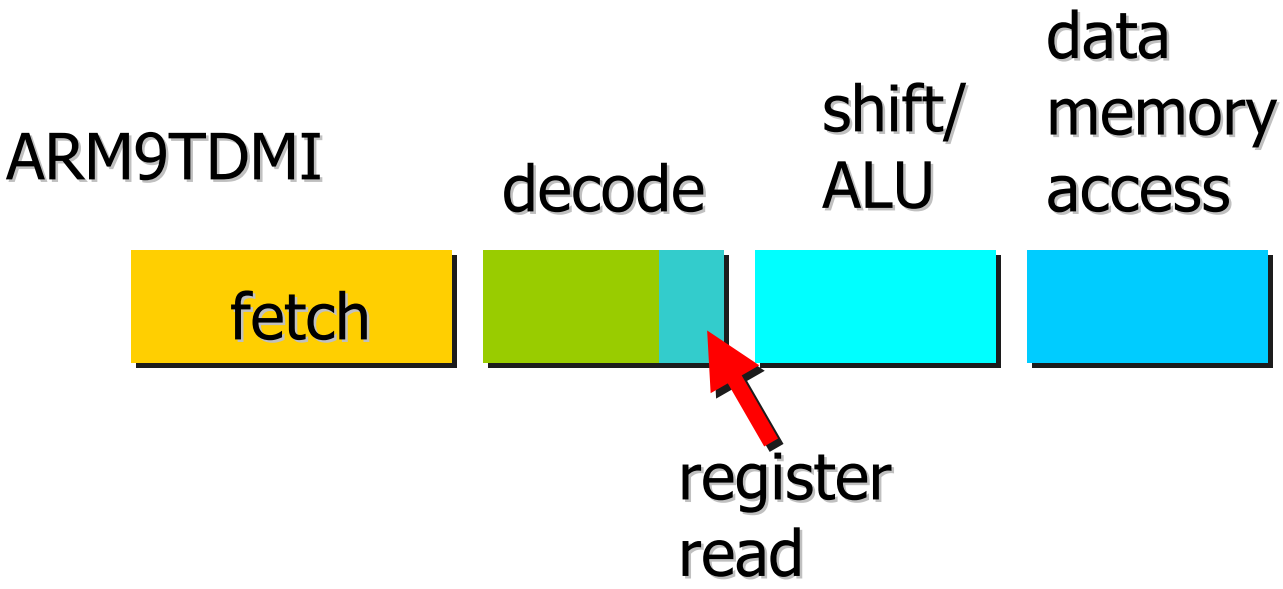

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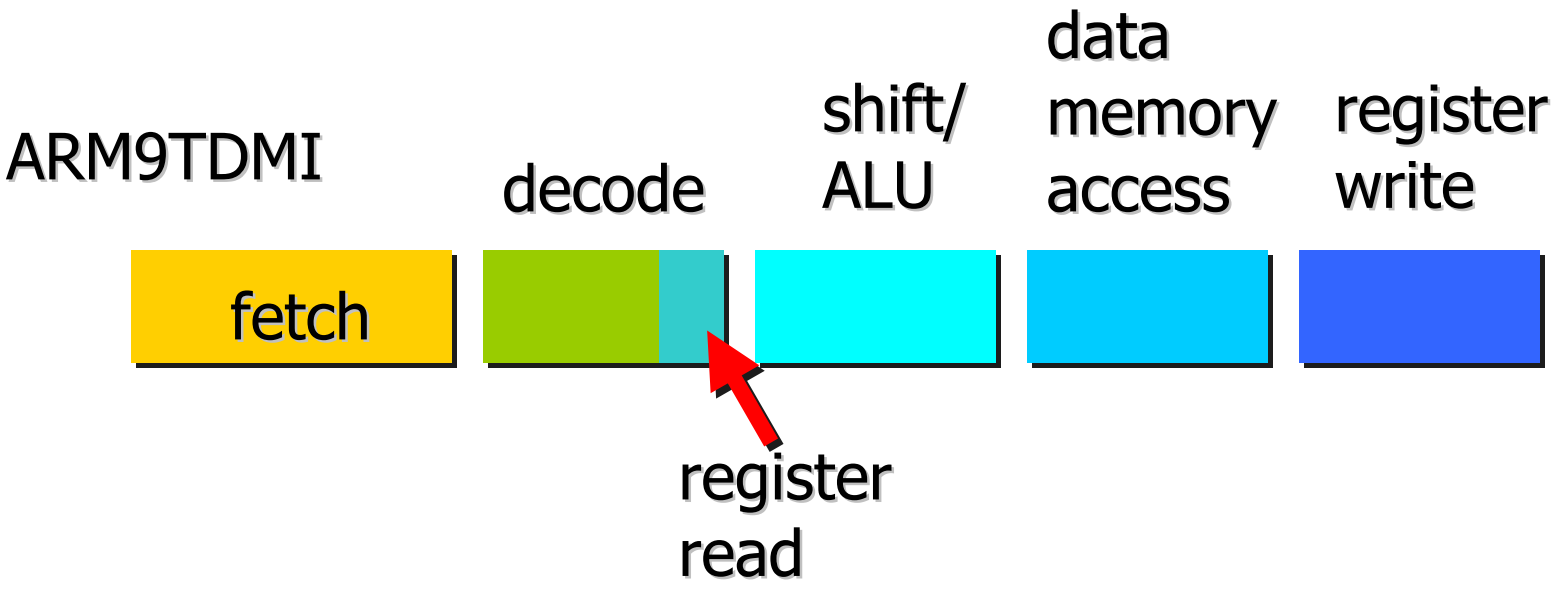

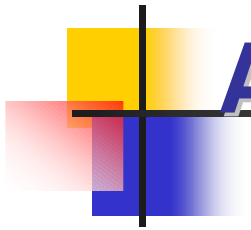

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- process: 0,25µm
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- Vdd: 2.5 V
- core area: 2.1 mm^2
- power: 150 mW

- transistors: 111 000
- clock: 0-200 MHz
- MIPS: 220
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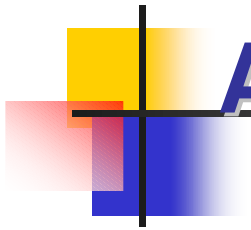

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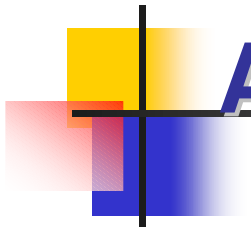

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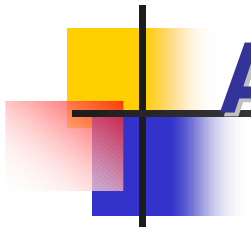

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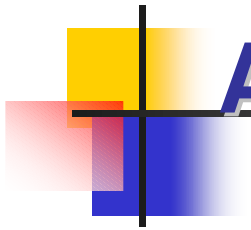

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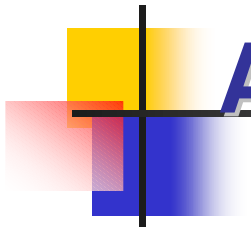

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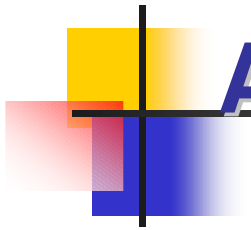

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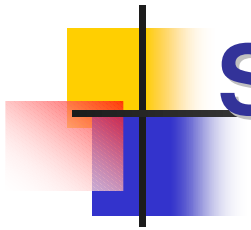

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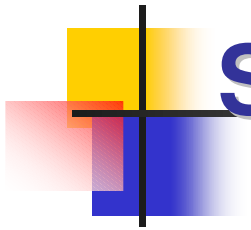

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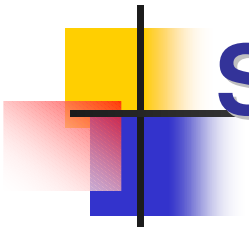

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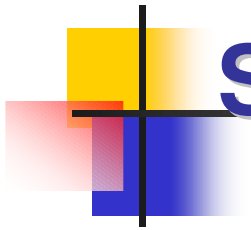

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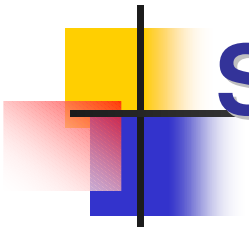

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