Digital Economy

Hardware foundries

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Implementation - Fabrication

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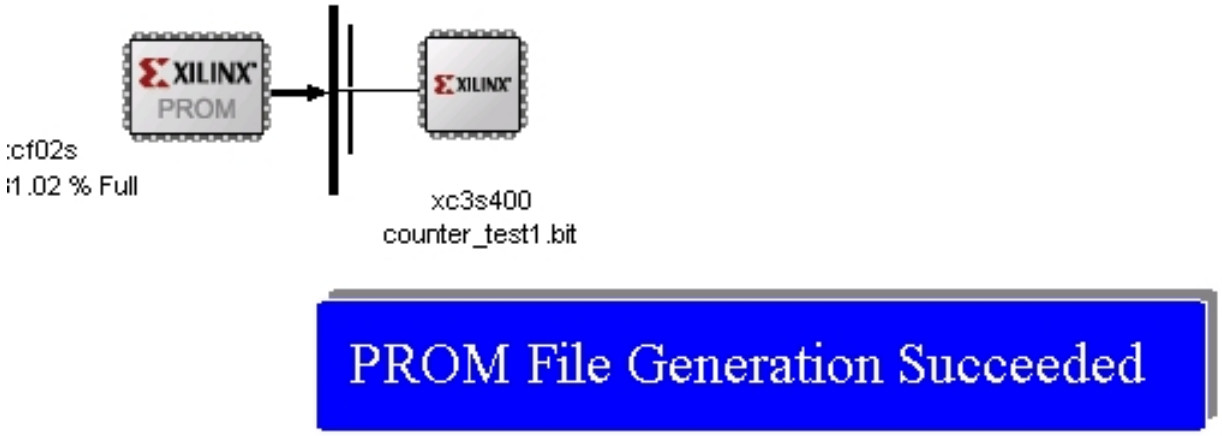
There are two implementation techniques for digital circuits/systems:

- through configurable circuits (firmware) : FPGA
- through application specific integrated circuits (hardware): ASIC

Firmware based implementation

- With firmware based implementation the virtual circuits/systems are mapped on configurable architectures.



Firmware based implementation

- This is done automatically via architecture synthesis tools.
- These tools are provided free of charge by the producers of configurable circuits.

Firmware implementation cost

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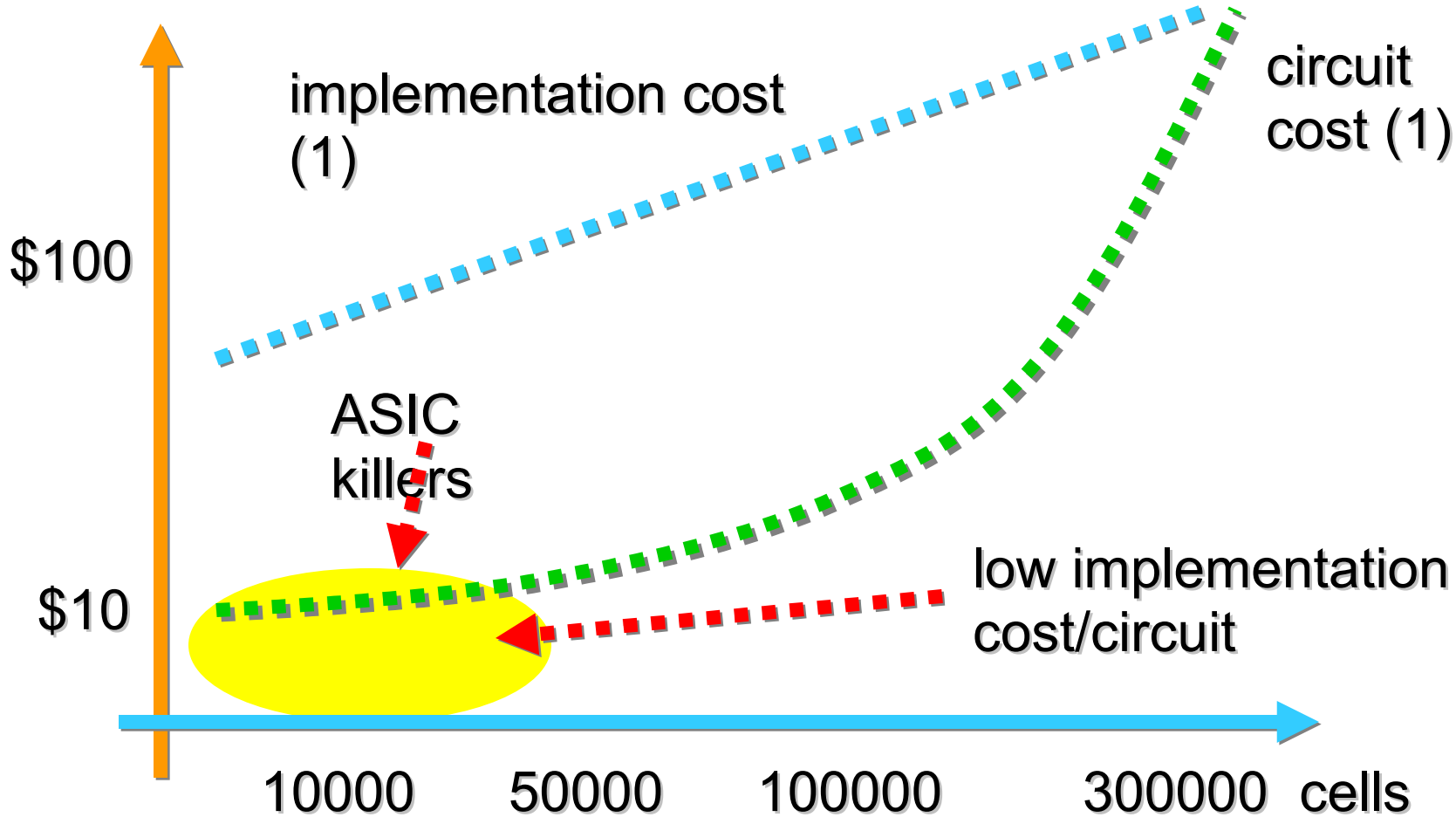
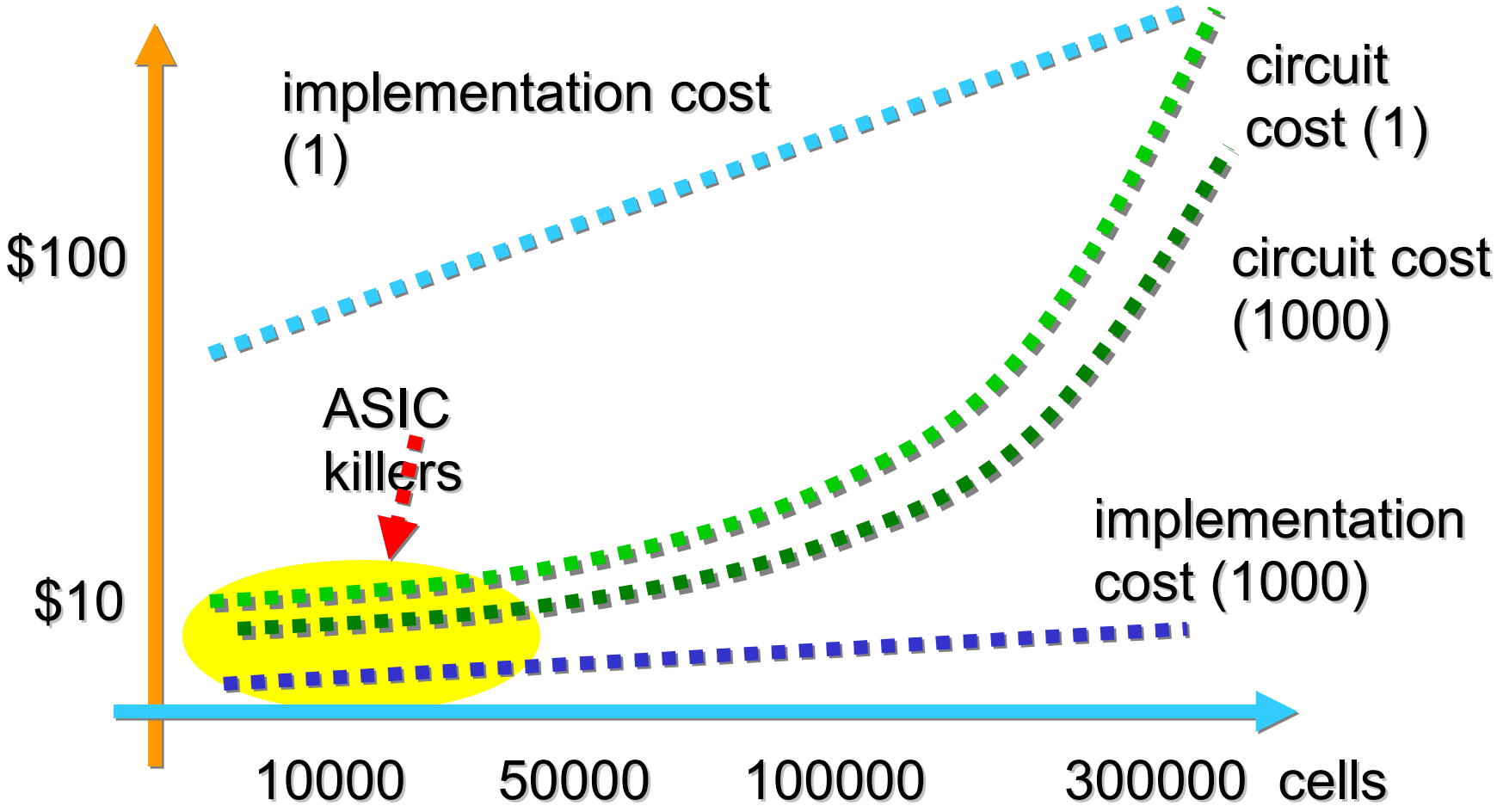
Essentially the mapping process is automated, however some decisions must be taken by the implementer (synthesis options, placement,..).

Firmware implementation cost



Firmware implementation cost



Firmware implementation cost

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Firmware implementation cost

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ISE *WebPACK* provides the tools and features along with the easy-to-use design environment and design tools providing instant access to the ISE features and functionality at no cost.

Hardware implementation cost

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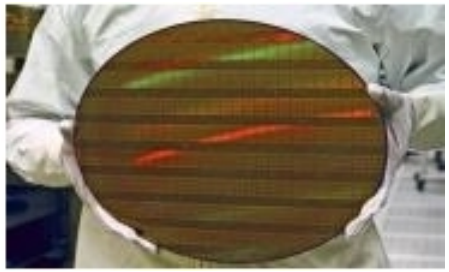
- physical (wafers) and chemical materials



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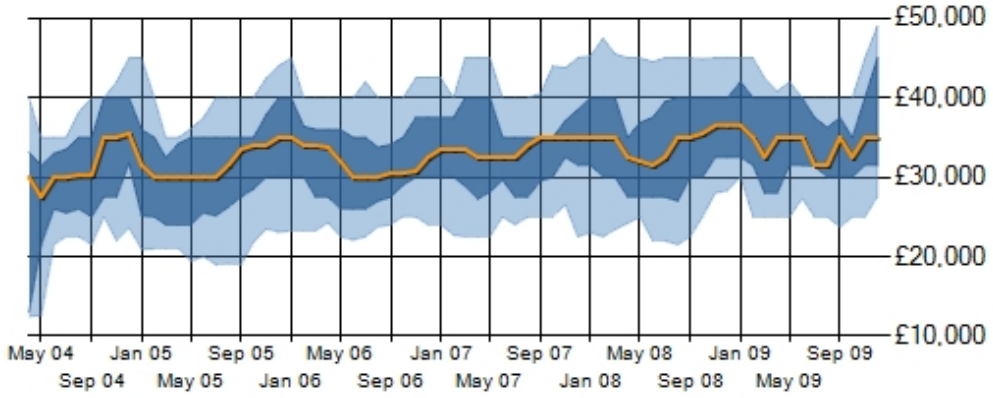
- computer equipment to design/map the HDL specifications on ASIC masks (layouts).
- fabrication equipment to project the layouts on silicon substrate – very high initial cost
- physical (wafers) and chemical materials
- design, implementation and test: labour cost (man-hours) – highly automated processes

electronic engineer salary UK



Hardware implementation cost

- The number of ASIC designs taping out in 2007 looks to be 3 275, down 4 percent from 2006's 3 408, according to market research company Gartner Inc.

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- of the 2007 ASIC design starts,

  about 200 starts made at 65-nanometer design rules

  or below.

Fab, design and R&D costs

	45-nm rule
Fab cost	$3B
Process R&D	$2.4B
Design cost	$20M-30M
Mask cost	$9M

Fab, design and R&D costs

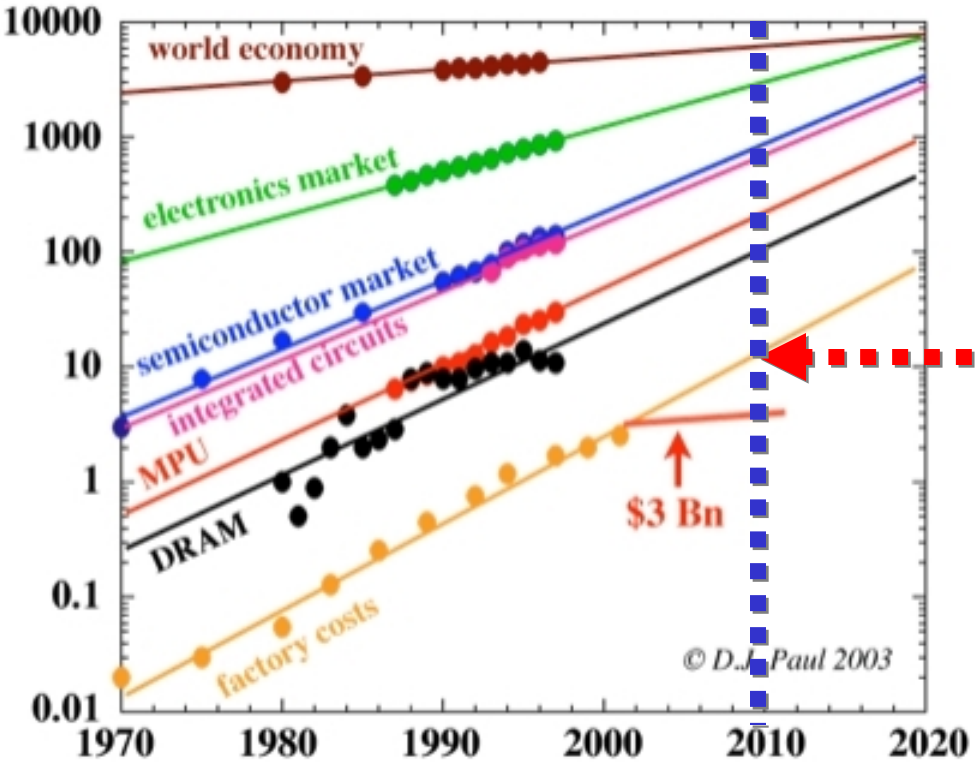
	45-nm rule	32-nm rule
Fab cost	$3B	$5B-10B
Process R&D	$2.4B	$3B
Design cost	$20M-30M	$75M
Mask cost	$9M	NA

4 years

Hardware implementation cost

- the requirements to develop next generation technology is one of the most pressing issues facing the industry, and one that could change the landscape of the world economy irrevocably.

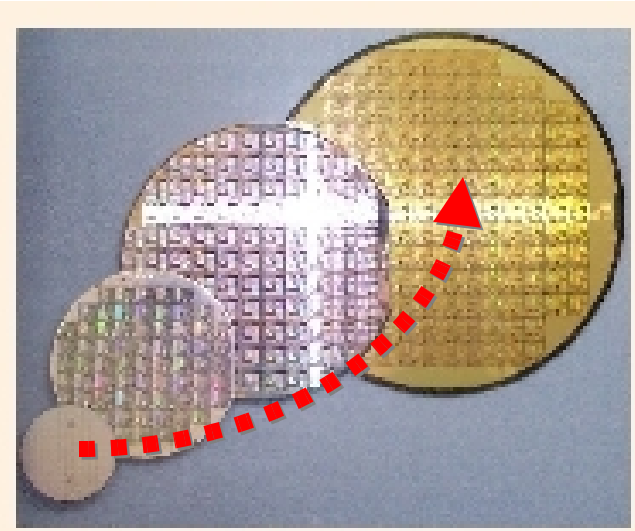
$ billions



we are here

Hardware implementation cost

- Moore's Law - which states that the number of transistors on a chip doubles every 18 months
- the increasing amount of innovation it supports has also spawned Moore's Law II.



Hardware implementation cost

- Moore's Law - which states that the number of transistors on a chip doubles every 18 months –
- the increasing amount of innovation it supports has also spawned Moore's Law II.
- the cost of building a manufacturing plant - otherwise known as a fab or a foundry - doubles every generation, which is currently around four years.

Hardware implementation cost

- Every time a new technology is implemented, a new fab has to be built.

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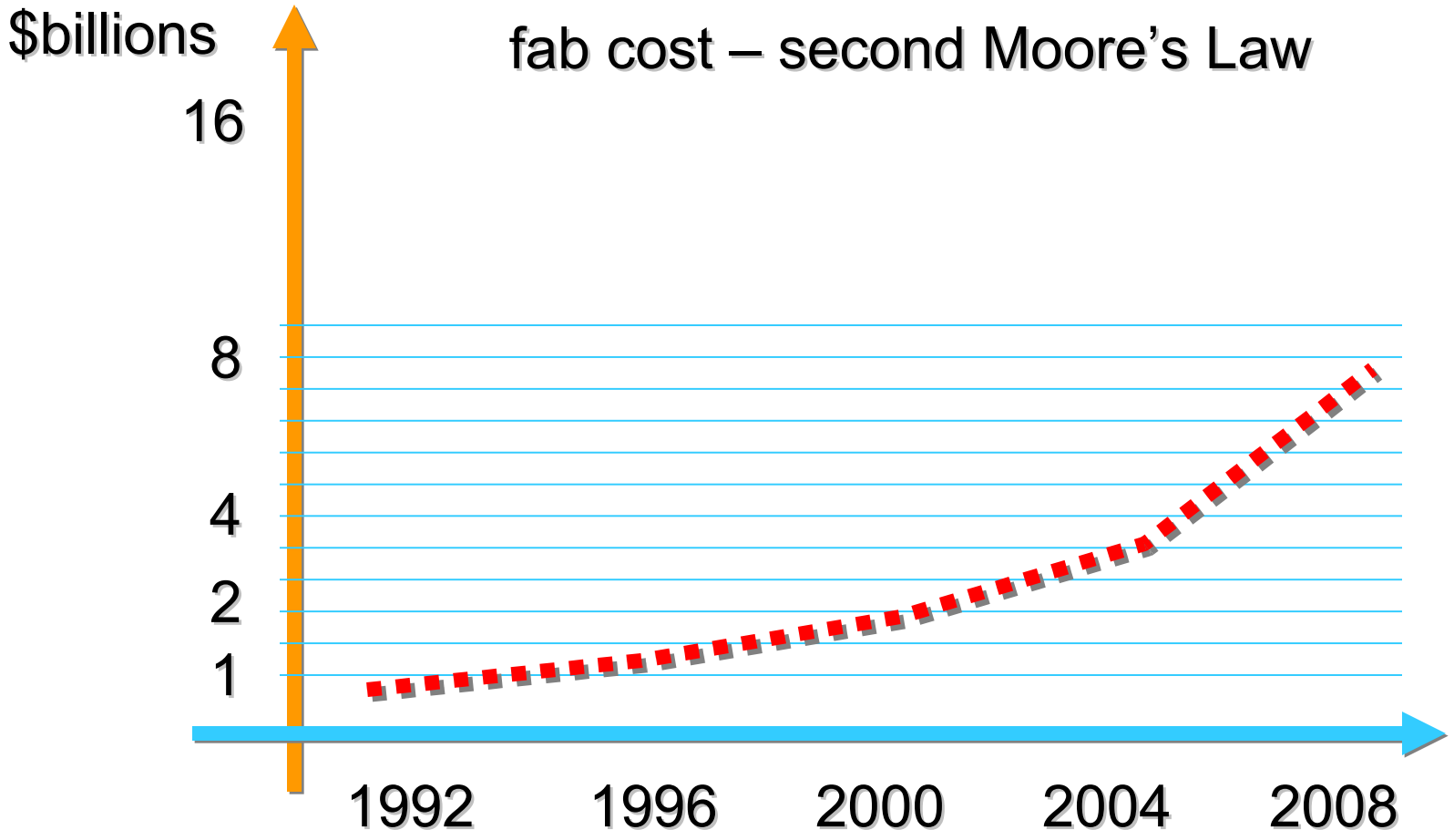
- Measures such as die shrinking, which allows more transistors to be packed on one chip, and increasing the wafer size - to produce more chips on one wafer - help to cut costs.
- As we go from 200mm to 300mm wafers, the cost structure improves by 35%.

Hardware implementation cost



Hardware implementation cost

Amortization scheme with:

- n=4 – total number of payments,
- r=0.04 – periodic interest rate
- A – periodic payment

Hardware implementation cost

Amortization scheme with:

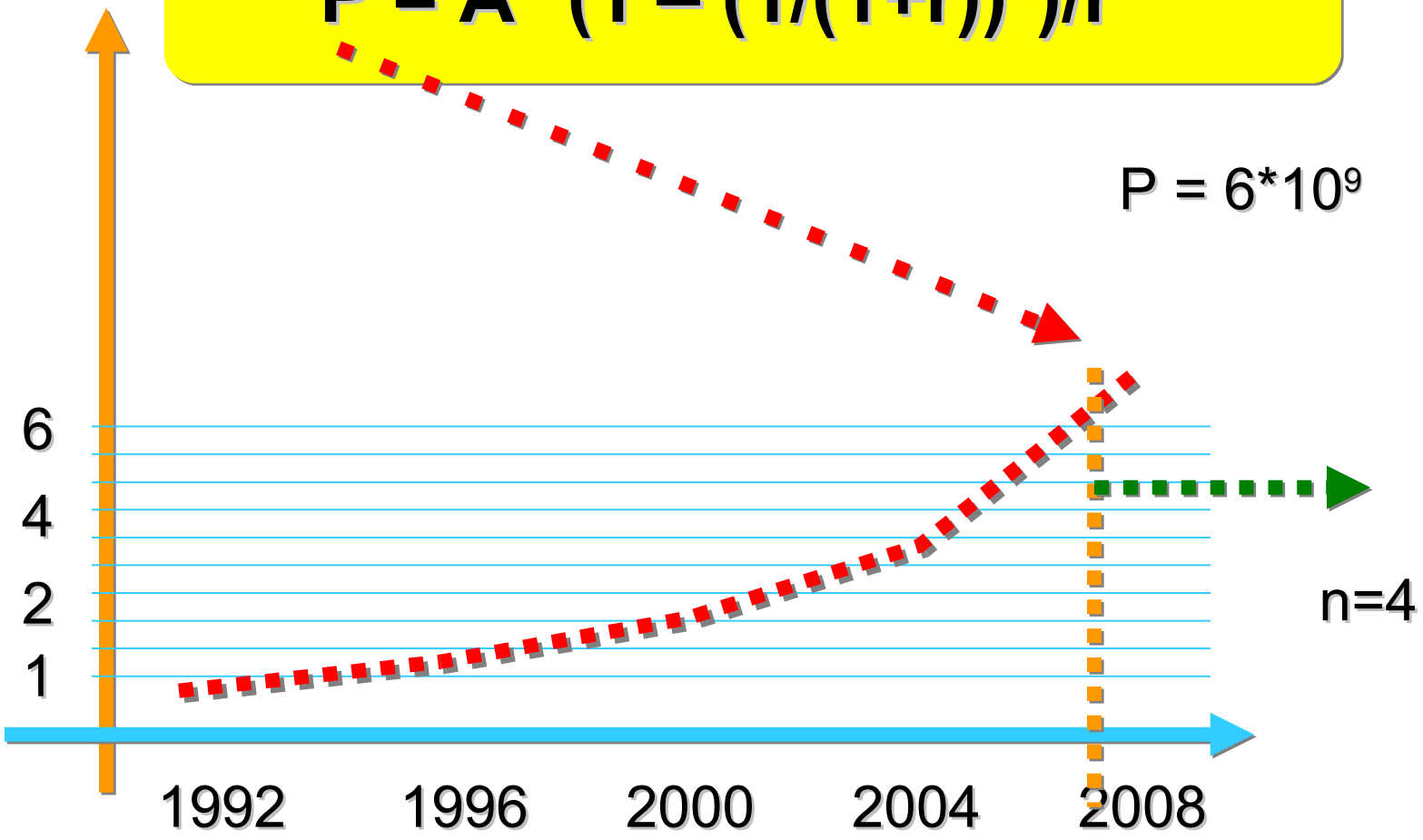
- n=4 – total number of payments,
- r=0.04 – periodic interest rate
- A – periodic payment/amortization rate

Foundry cost – investment loan (dollars):

$$P = 6*10^9$$

Hardware implementation cost

$$P = A^* (1 - (1/(1+r))^n)/r$$



Hardware implementation cost

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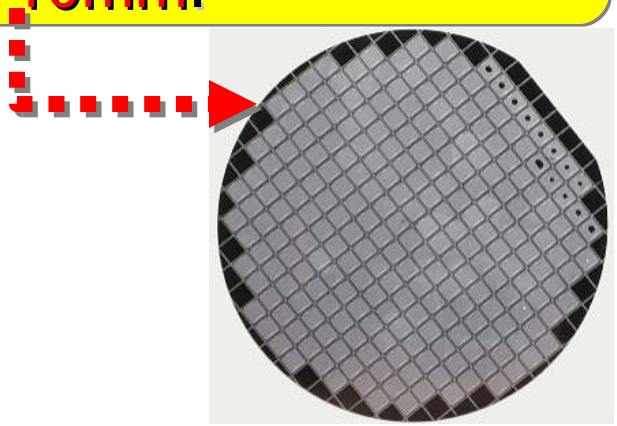
- To simplify the calculation, we decide to produce only one type of circuits.

- The price of the circuit is fixed to $50 each.

So we take $5 from each circuit!

Hardware implementation cost

- Each circuits is a part of a wafer; let us suppose that the size of the circuit (die) is 10mm*10mm.

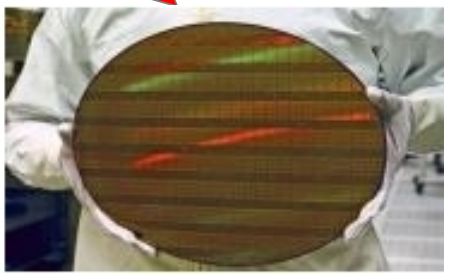


10mm*10mm

Hardware implementation cost

- Each circuits is a part of a wafer; let us suppose that the size of the circuit is 10mm*10mm.

- The diameters of wafers are: 200 mm and 300 mm



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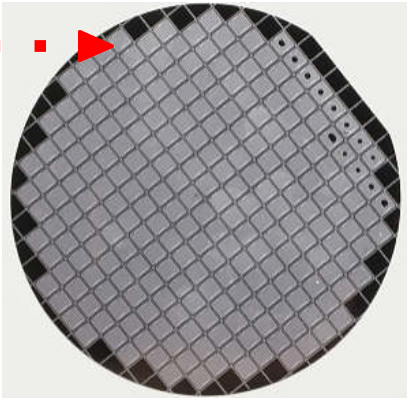


- Calculate how many wafers must be produced a year to cover the amortization expense ?
- Do the same calculation for 200mm and 300mm wafers.

Hardware implementation cost

Wafer diameter in mm:
d1 = 200 mm
d2 = 300 mm

Hardware implementation cost

Wafer diameter in mm:

d1 = 200 mm

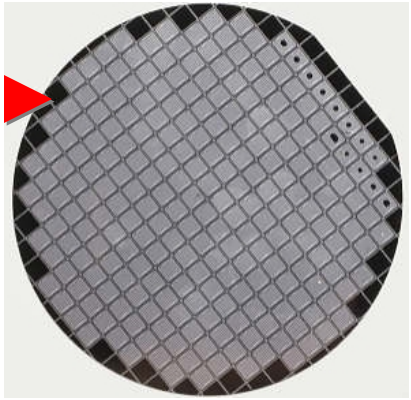
d2 = 300 mm

Effective number of dies on a wafer:

π *(wafer_diameter/2)^2/die_area –

π *wafer_diameter/(2*die_area)$^{0.5}$=

these parts are not used



Hardware implementation cost

Effective number of dies on a wafer:

$\pi*(\text{wafer_diameter}/2)^2/\text{die_area} - \pi*\text{wafer_diameter}/(2*\text{die_area})^{0.5}=$

$\pi*(200/2)^2/100 - \pi*200/(2*100)^{0.5}=$ nd1

$\pi*(300/2)^2/100 - \pi*300/(2*100)^{0.5}=$ nd2

nd1 – number of dies on 200 mm wafer

nd2 – number of dies on 300 mm wafer

Hardware implementation cost

Effective number of dies on a wafer:

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π*(200/2)^2/100 – π*200/(2*100)$^{0.5}$= nd1

π*(300/2)^2/100 – π*300/(2*100)$^{0.5}$= nd2

Each die price is $50 ; 10% of this is taken for amortization - it is $5

Hardware implementation cost

It gives us:

- nd1 circuits per 200 wafer*$5 =
- nd2 circuits per 300wafer*$5 =

from

$$\mathbf{P = A^* (1 - (1/(1+r))^n)/r}$$

we get:

$$\mathbf{A = P^*r/ (1 - (1/(1+r))^n)=}$$

for: n=4, r=0.04, and $P=\$6*10^9$

Hardware implementation cost

The answer is:

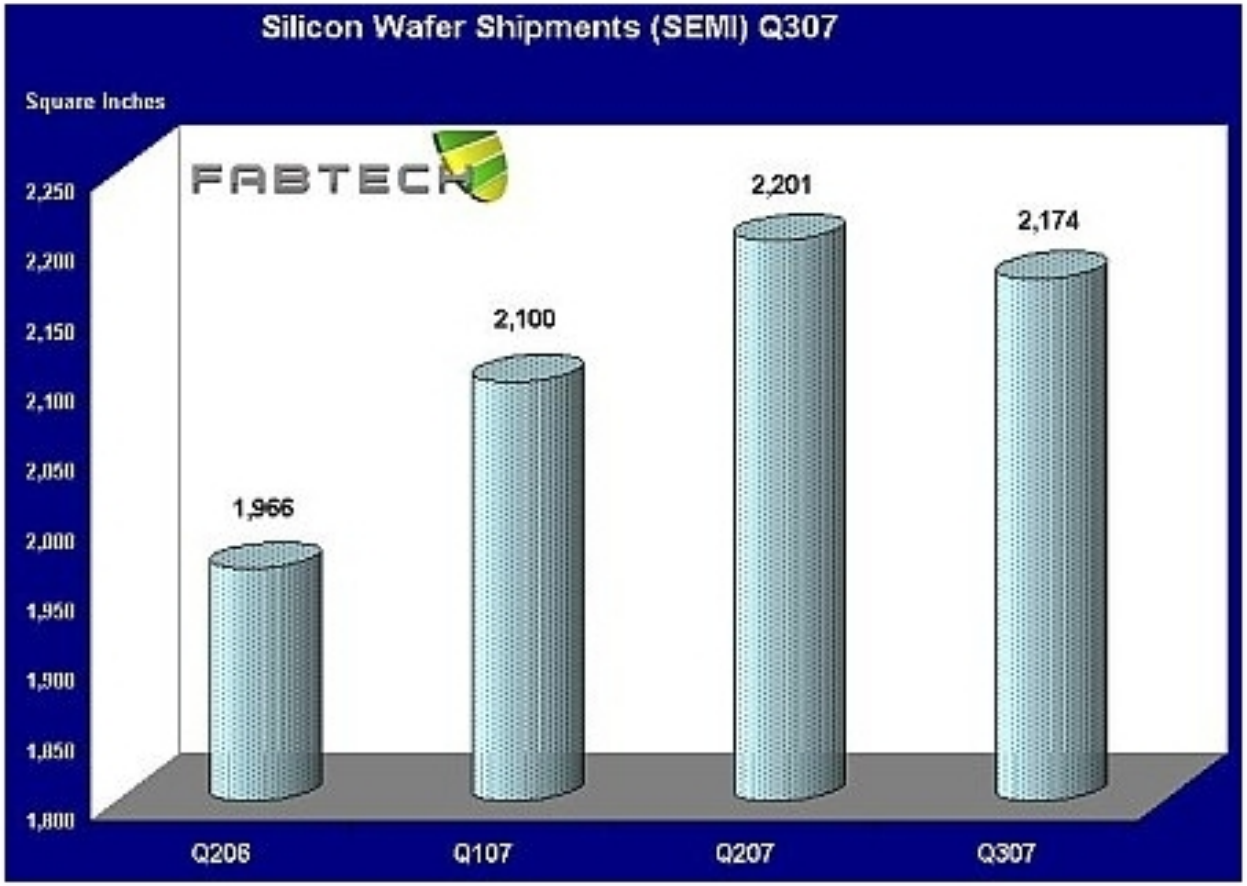
amortization payment / nd1 = x wafers
amortization payment / nd2 = y wafers

Note:

- global daily production of all kinds of silicon wafers is about 200 000 units (8”, 15”, 20”, 30”)
- only in China there is about 50 foundries

Hardware implementation cost

Total silicon wafer area shipments were 2174 million square inches in 3Q07 compared to 2201 in 2Q07.



Hardware implementation cost

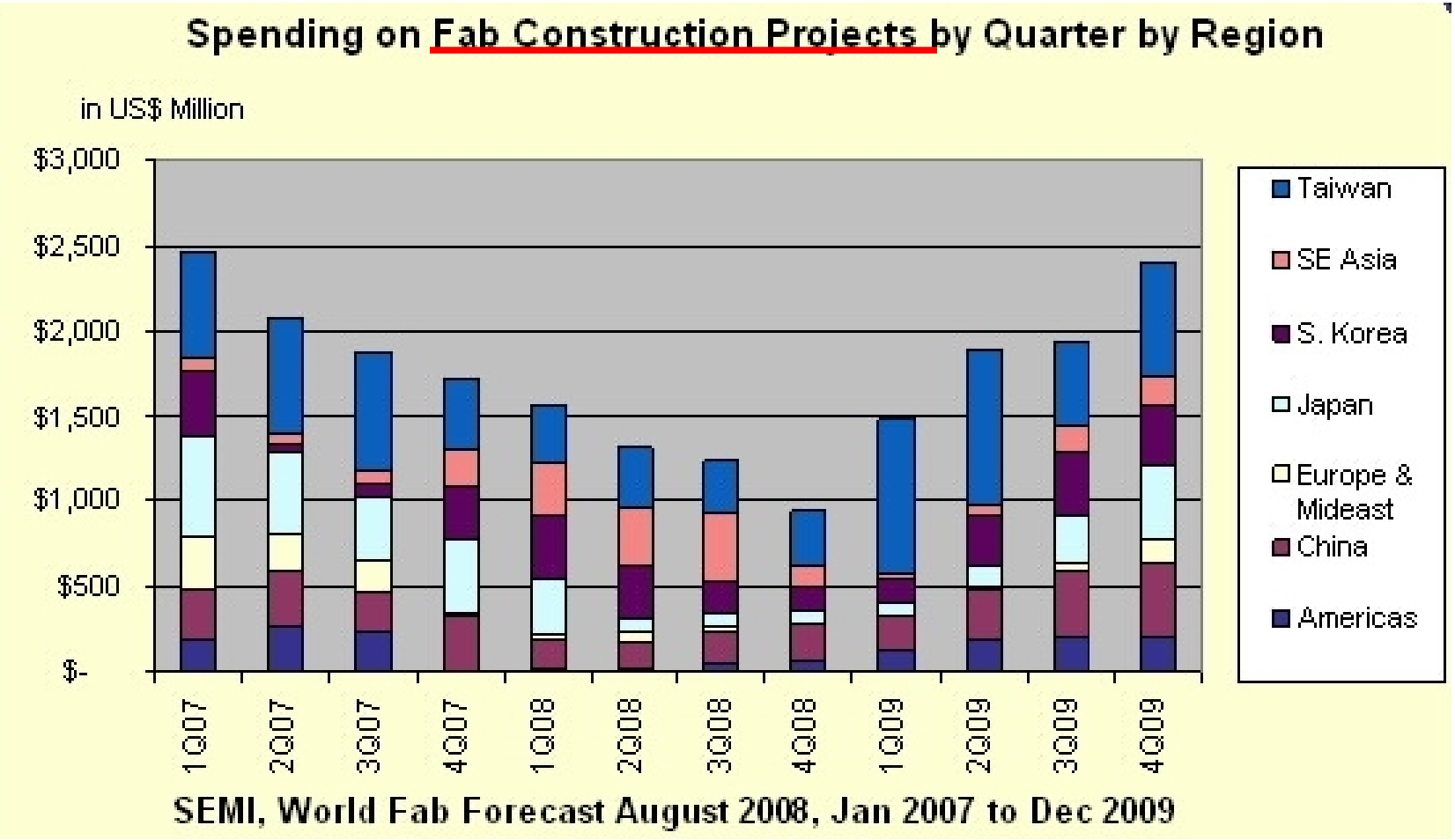
Global H1 2009 Pure-Play Foundry Revenues by Company

(Millions of Dollars)

Rank	Company	Revenue	Percent of Market	Cumulative Percentage
1	TSMC	$3,300	47.7%	47.7%
2	Globalfoundries*	$1,159	16.7%	64.4%
3	UMC	$1,009	14.6%	79.0%
4	Semiconductor Manufacturing International Corp (SMIC)	$368	5.3%	84.3%
	Others	**$1,084**	**15.7%**	**100.0%**
	Total	**$6,920**	**100.0%**	

2009 – H1 first half,
Globalfoundries - former Chartered (Singapore)

Hardware implementation cost



Fabless companies

- We estimate that foundries will have contributed between 10% and 11% of all the designed chips produced by the end of 2006.

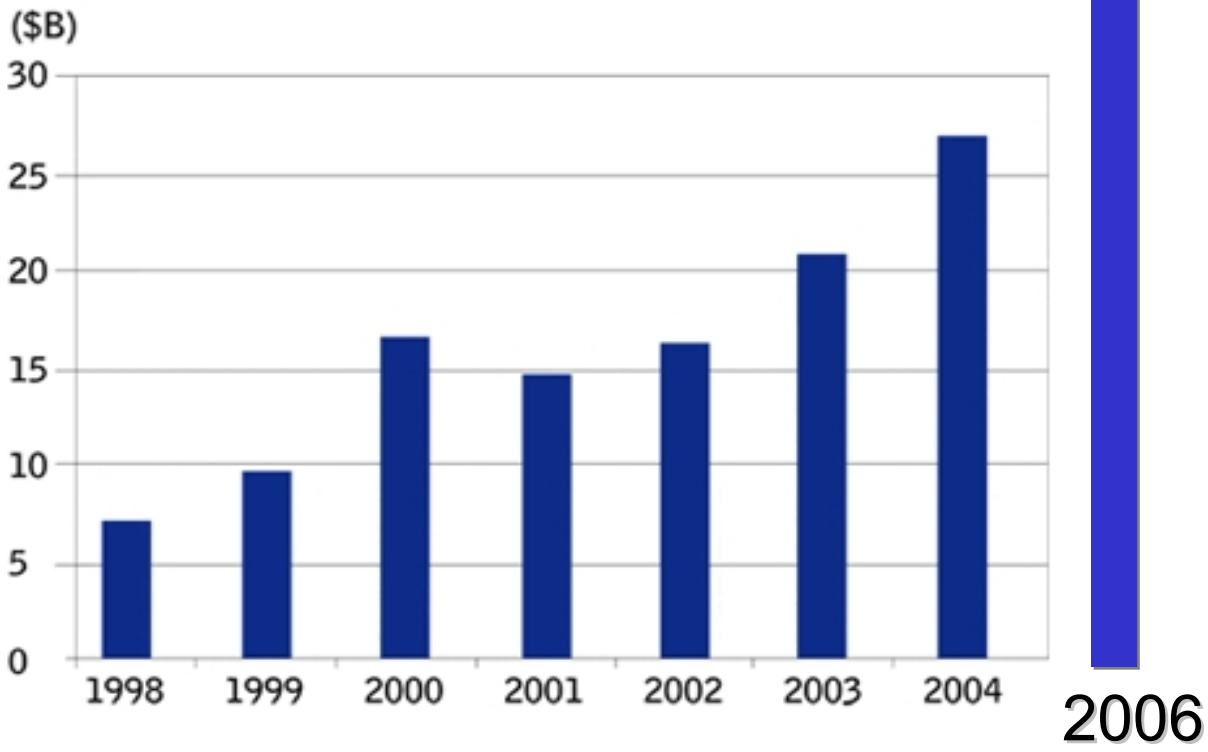
All other chip designs were provided by fabless companies.

- Nowadays the investment cost of building foundries becomes prohibitive for traditional chip designers and manufacturers (USA and Europe).

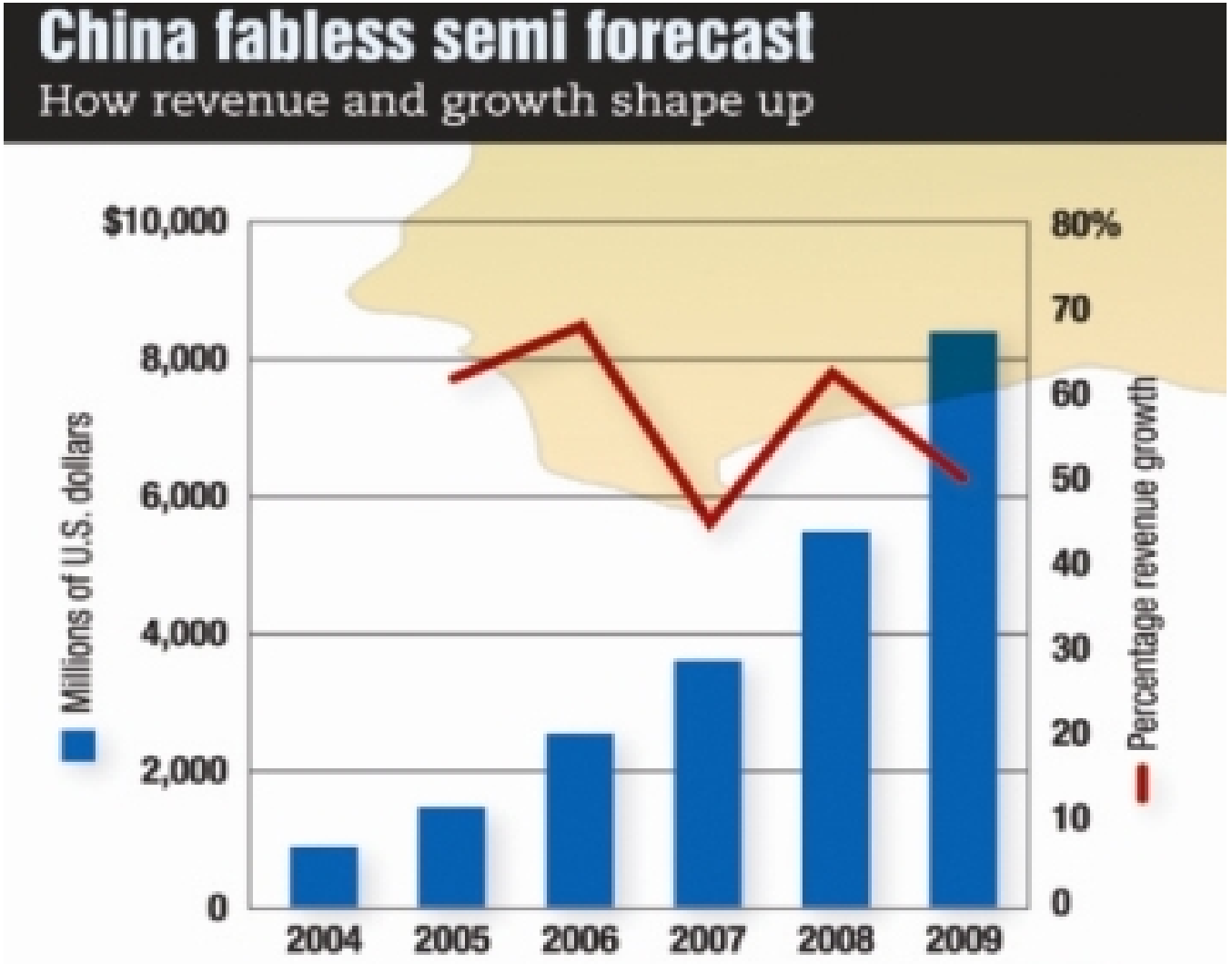
Fabless companies

Fabless IC company sales increased sixfold from $7.3 billion to $42.3 billion (1998-2006)

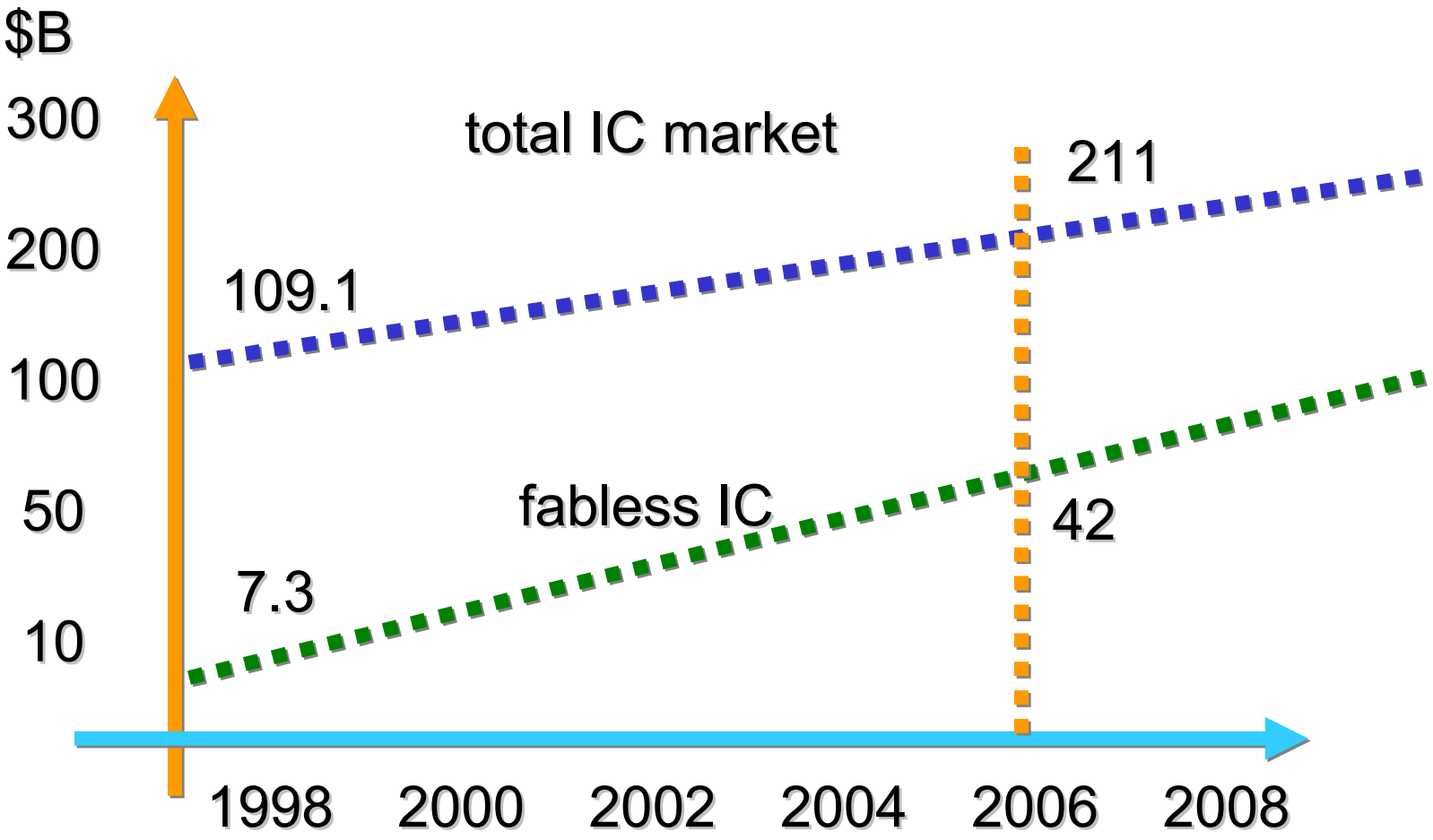
The total IC market increased only 93 percent over from $109.1 billion to $211 billion.



Fabless companies - China



Fabless part of IC industry



Semiconductor (chips) sales

2Q09 Top 20 Semiconductor Sales Leaders ($M)

2Q09 Rank	1Q09 Rank	2008 Rank	Company	Headquarters	2008 Tot Semi	08/07 % Change	1Q09 Tot Semi	2Q09 Tot Semi	2Q09/1Q09 % Change
1	1	1	Intel	U.S.	34,490	-2%	6,573	7,382	12%
2	2	2	Samsung	South Korea	20,272	2%	3,686	4,767	29%
3	3	5	Toshiba	Japan	10,422	-12%	2,008	2,310	15%
4	4	3	TI	U.S.	11,618	-13%	1,939	2,285	18%
5	10	4	TSMC*	Taiwan	10,556	8%	1,162	2,238	93%
6	5	6	ST	Europe	10,325	3%	1,657	1,993	20%
7	6	8	Qualcomm**	U.S.	6,477	15%	1,316	1,786	36%
8	8	7	Renesas	Japan	7,017	-12%	1,233	1,381	12%
9	7	9	Sony	Japan	6,420	-11%	1,270	1,360	7%
10	13	10	Hynix	South Korea	6,182	-33%	927	1,301	40%
11	11	14	Micron	U.S.	5,688	3%	1,020	1,225	20%
12	9	12	AMD	U.S.	5,808	-1%	1,177	1,184	1%
13	12	11	Infineon	Europe	5,903	2%	970	1,150	19%
14	14	13	NEC	Japan	5,732	2%	863	1,005	16%
15	16	18	Broadcom**	U.S.	4,509	20%	827	966	17%
16	15	19	Panasonic	Japan	4,321	13%	850	920	8%
17	19	25	MediaTek**	Taiwan	2,845	16%	704	847	20%
18	21	20	Nvidia**	U.S.	4,959	-11%	597	795	33%
19	20	15	NXP	Europe	5,020	-14%	648	788	22%
20	18	16	Freescale	U.S.	4,959	-11%	798	784	-2%
—	—	—	Total Top 20	—	173,523	—	30,225	36,467	21%

*Foundry **Fabless

Source: IC Insights, company reports

Summary

- form concept to product
- design and reuse
- firmware based implementation
- hardware based implementation
- hardware implementation cost
- fabless companies